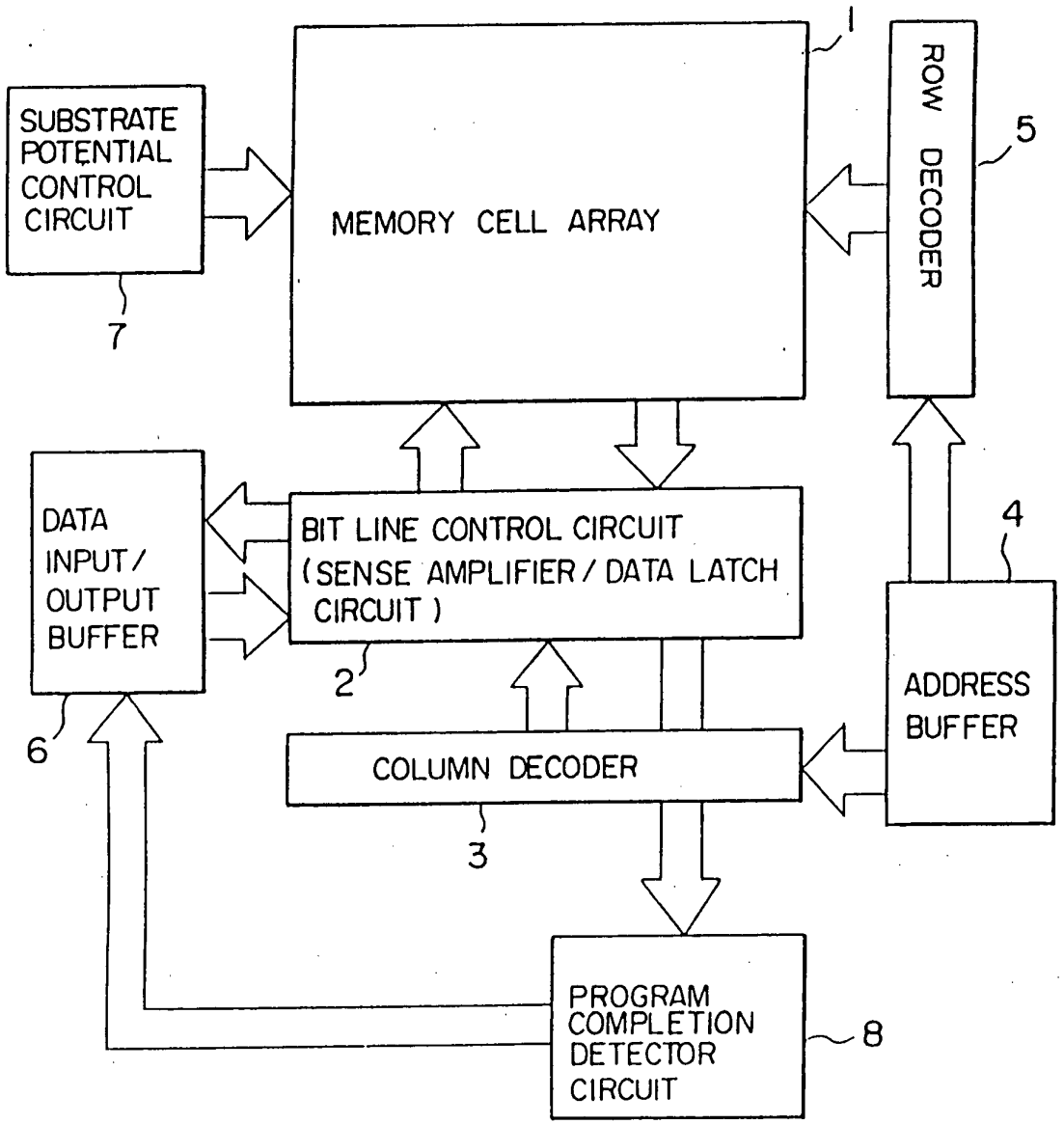

SUBSTRATE POTENTIAL CONTROL CIRCUIT
7
MEMORY CELL ARRAY
1
ROW DECODER
5
DATA INPUT/ OUTPUT BUFFER
6
BIT LINE CONTROL CIRCUIT (SENSE AMPLIFIER / DATA LATCH CIRCUIT)
2
4
ADDRESS BUFFER
COLUMN DECODER
3
PROGRAM COMPLETION DETECTOR CIRCUIT
8

FIG. 1

FIG. 2(a)

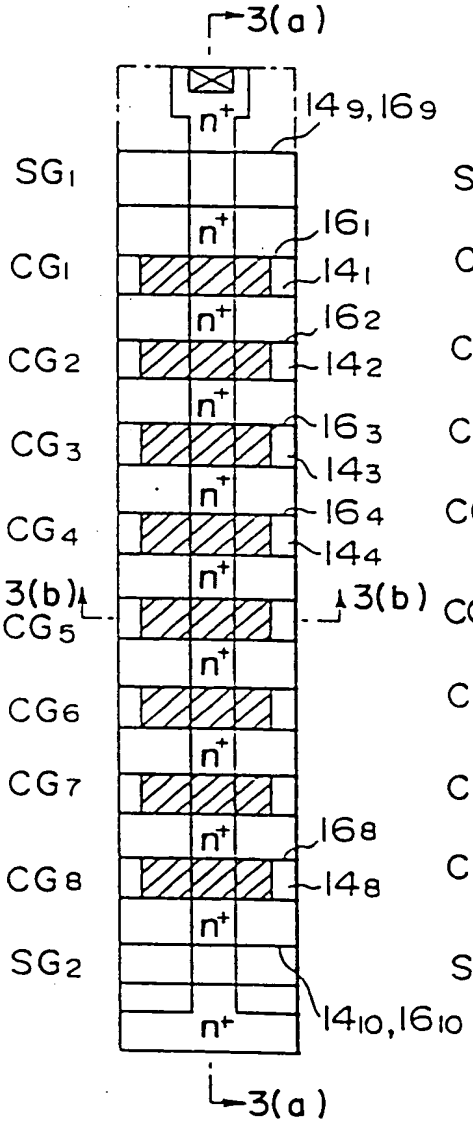

3(a)
n+
149, 169
SG1
161
CG1
141
162
CG2
142
163
CG3
143
164
CG4
144
3(b)
CG5
3(b)
CG6
CG7
168
CG8
148
SG2
1410, 1610
3(a)

FIG. 2(b)

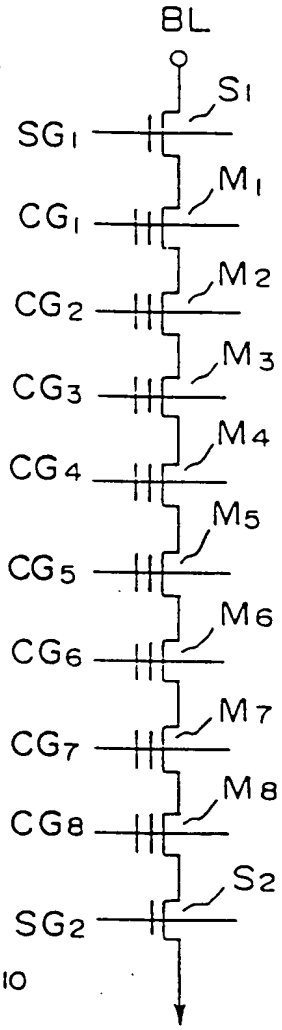

BL
S1
SG1
M1
CG1
M2
CG2
M3
CG3
M4
CG4
M5
CG5
M6
CG6
M7
CG7
M8
CG8
S2
SG2

FIG. 3(a)

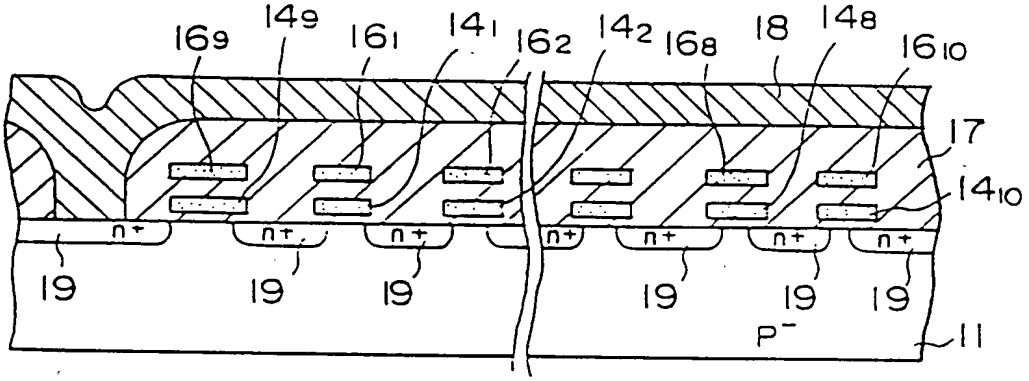
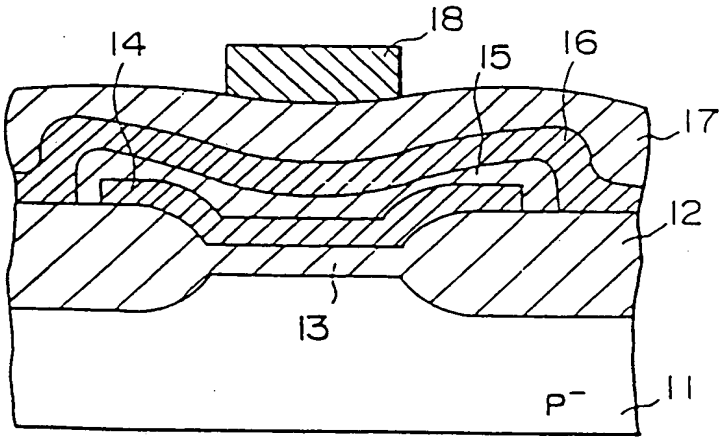

16₉
14₉
16₁
14₁
16₂
14₂
16₈
18
14₈
16₁₀
17
14₁₀
n+
19
P⁻
11

FIG. 3(b)


18
14
15
16
17
12
13
P⁻
11

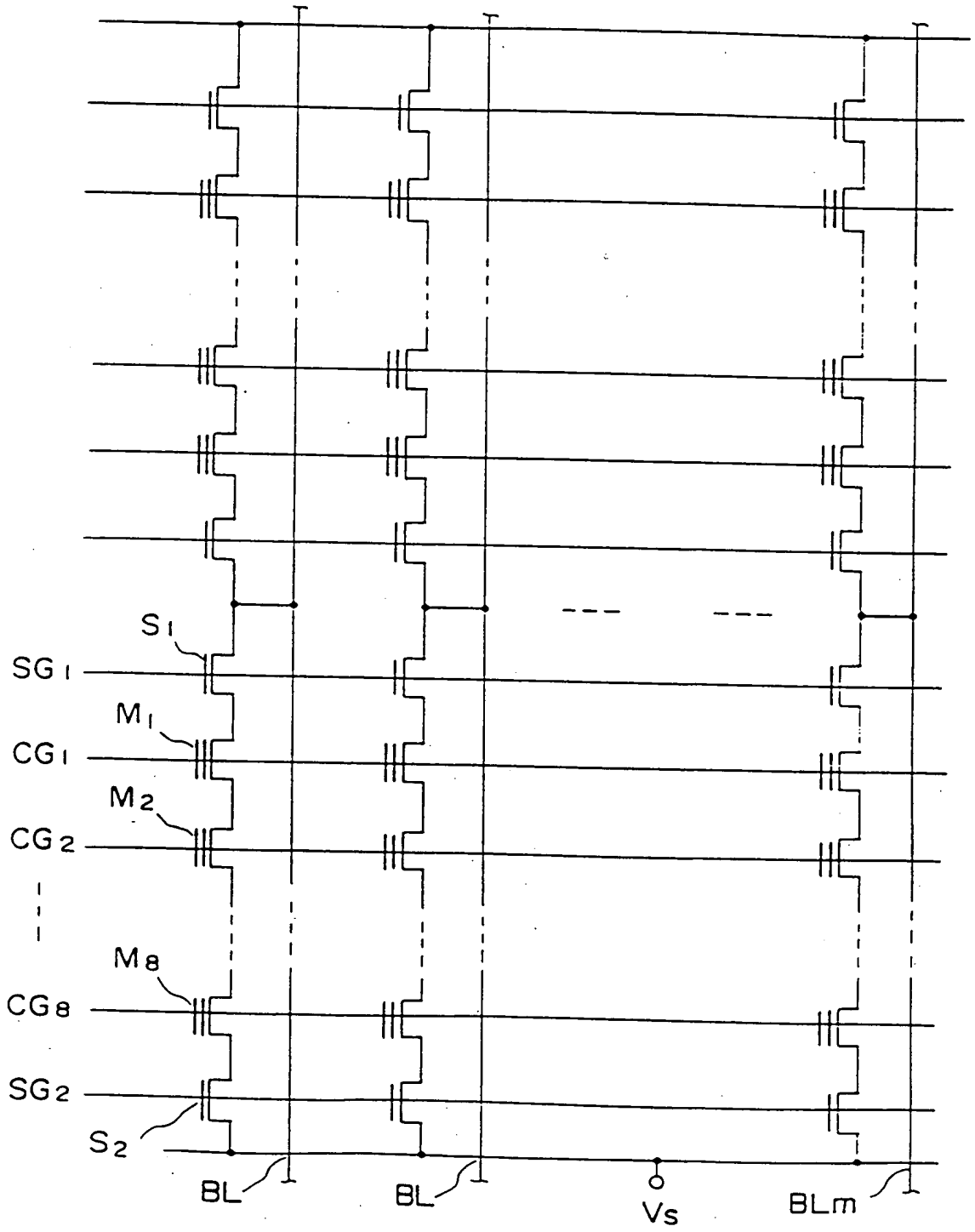


FIG. 4

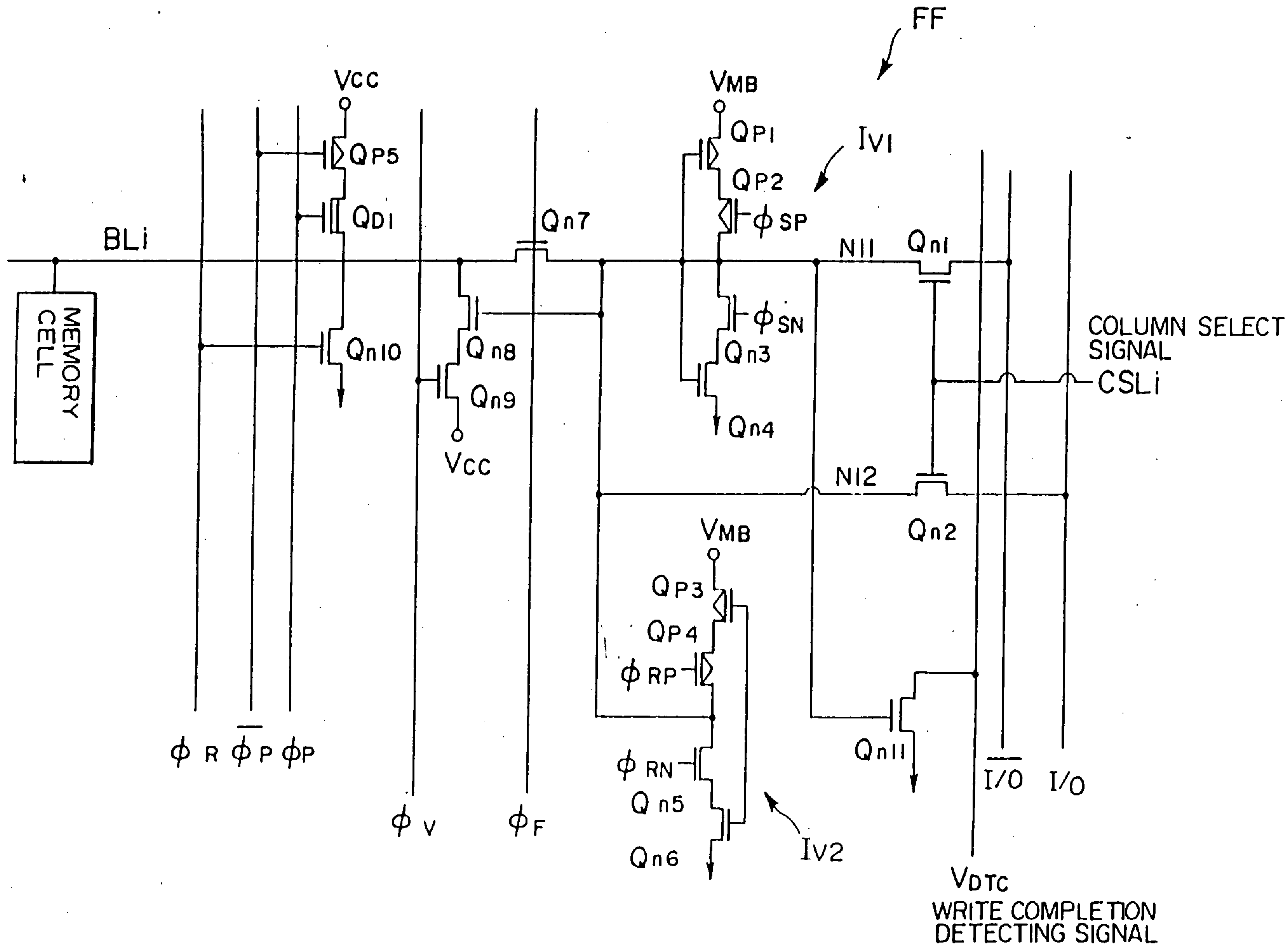

FF
VCC
QP5
QD1
Qn10
MEMORY CELL
BLi
Qn7
Qn8
Qn9
VCC
VMB
QP1
QP2
ϕSP
IV1
ϕSN
Qn3
Qn4
N11
Qn1
COLUMN SELECT SIGNAL
CSLi
N12
Qn2
VMB
QP3
QP4
ϕRP
ϕRN
Qn5
Qn6
IV2
Qn11
ϕR
ϕ̄P
ϕP
ϕV
ϕF
I/O
I/O
VDTC
WRITE COMPLETION DETECTING SIGNAL

FIG. 5

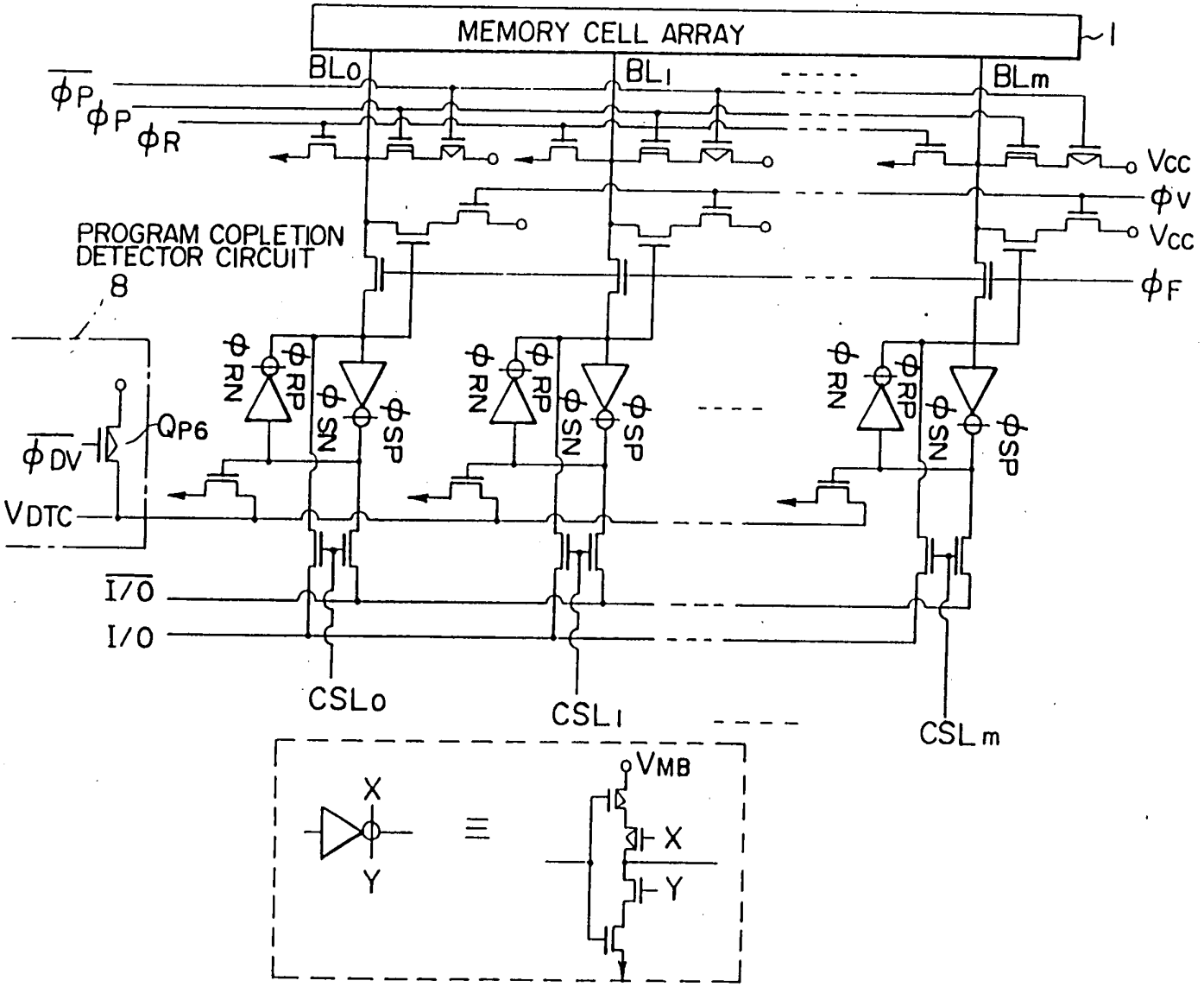

MEMORY CELL ARRAY
1
BLo
BL1
BLm
φP
φP
φR
Vcc
φv
Vcc
φF
PROGRAM COPLETION
DETECTOR CIRCUIT
8
φRN
φRP
φSN
φSP
QP6
φDV
VDTC
I/O
I/O
CSLo
CSL1
CSLm
VMB
X
Y
≡

FIG. 6

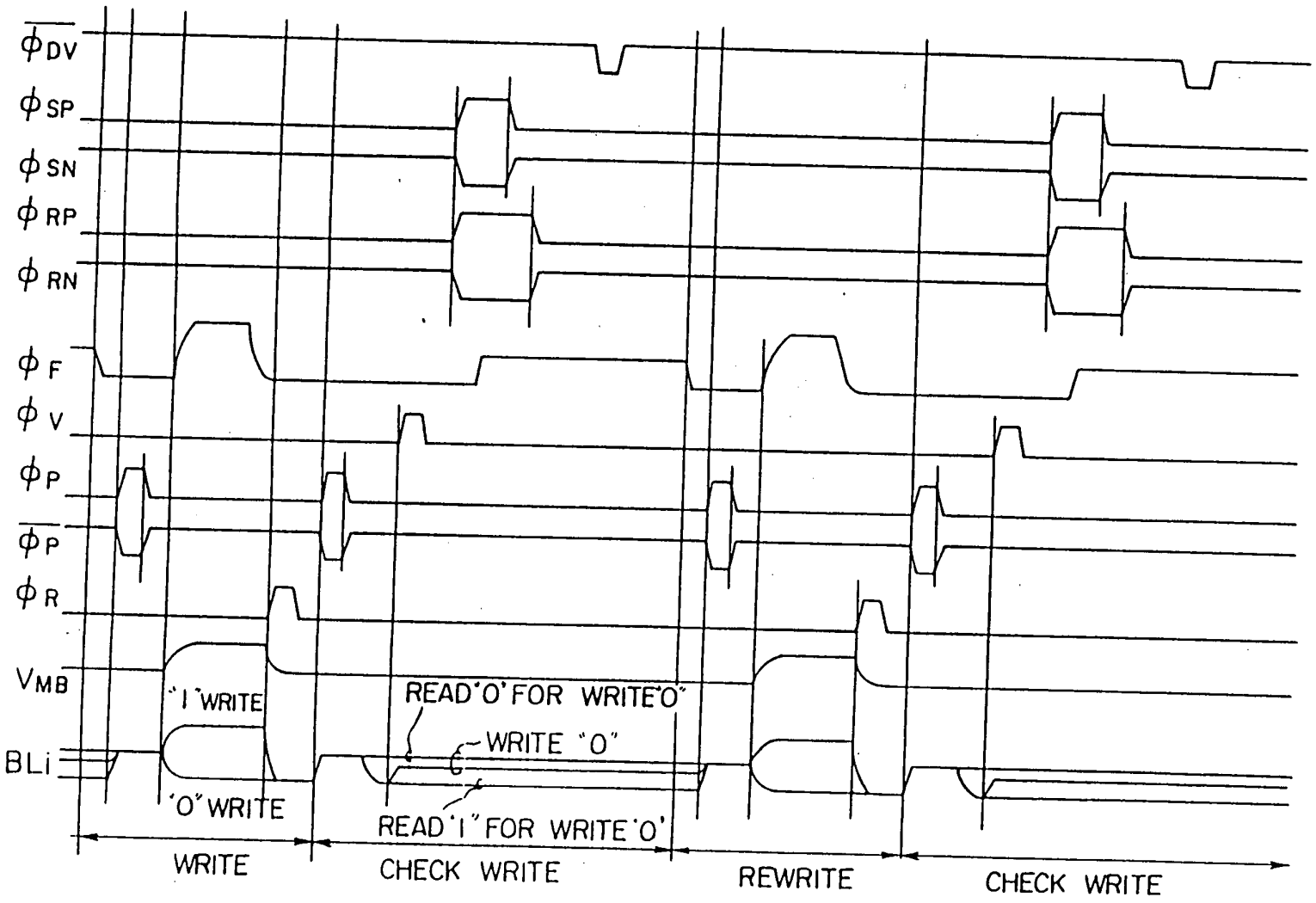


FIG. 7

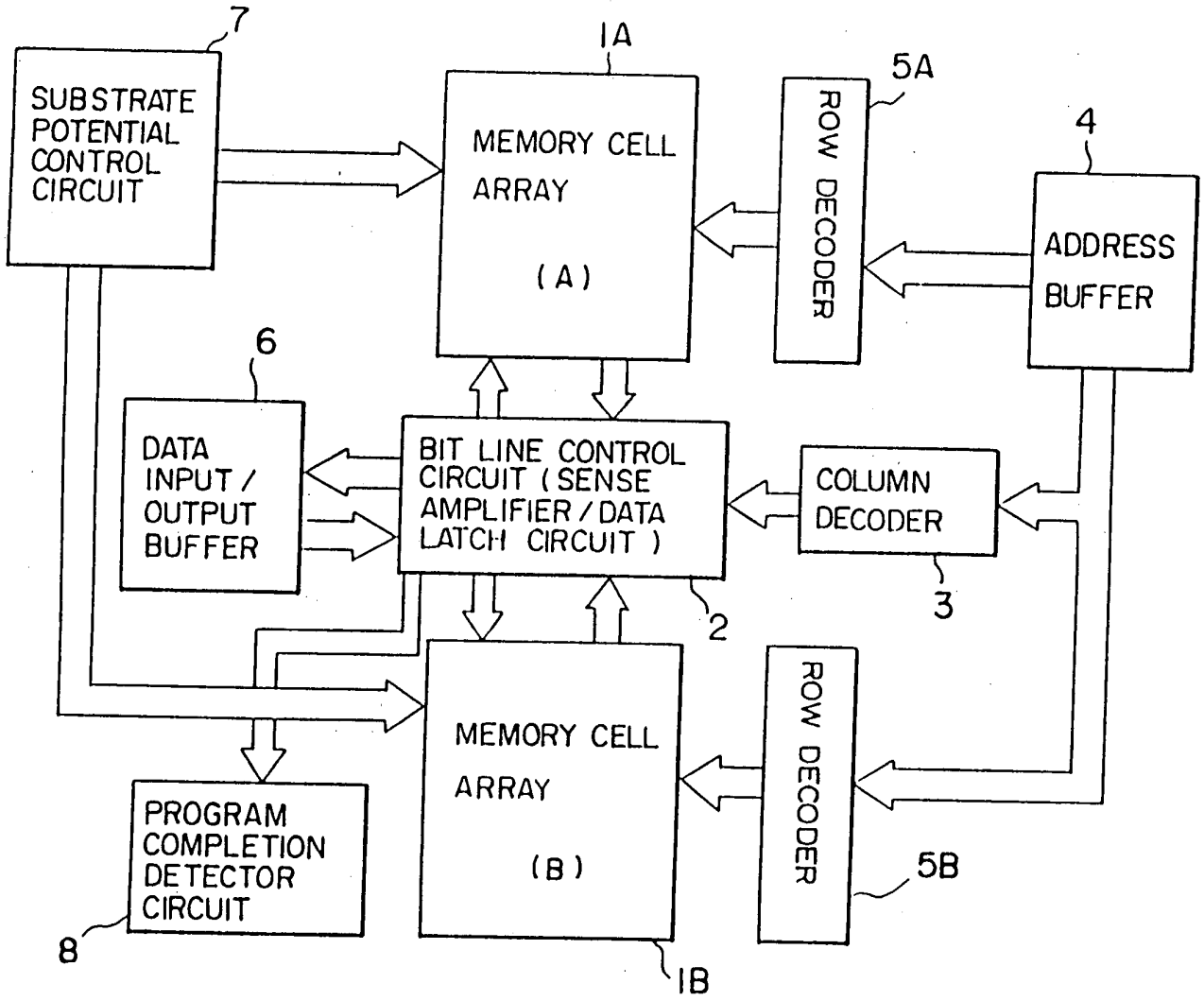


FIG. 8

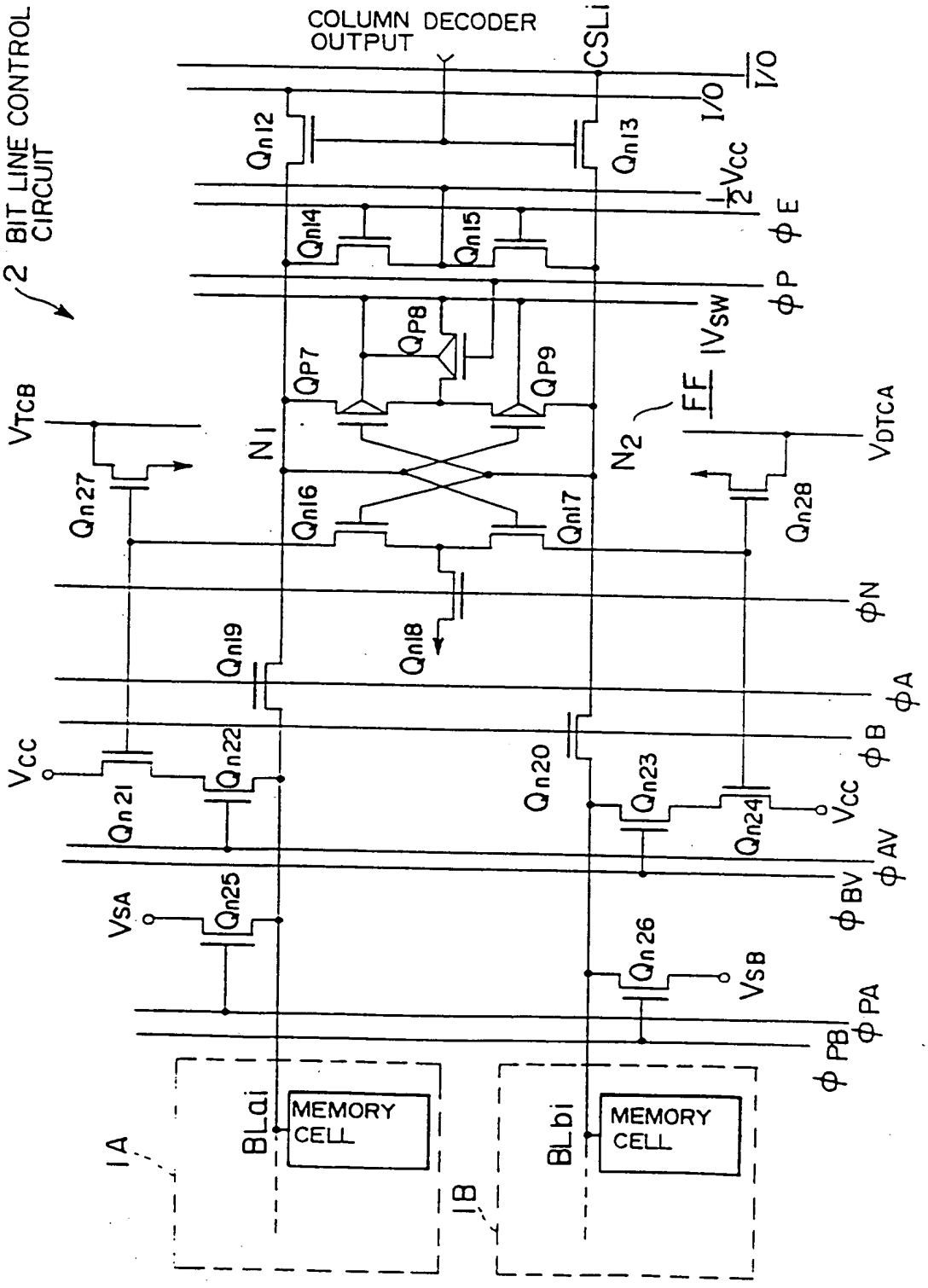

2 BIT LINE CONTROL CIRCUIT
COLUMN DECODER OUTPUT
CSLi
I/O
$\overline{I/O}$
$\frac{1}{2}V_{CC}$
ϕE
ϕP
V_{SW}
V_{TCB}
V_{DTCA}
FF
N1
N2
ϕN
ϕA
ϕB
ϕAV
ϕBV
ϕPA
ϕPB
V_{CC}
V_{SA}
V_{SB}
Qn12
Qn13
Qn14
Qn15
QP7
QP8
QP9
Qn16
Qn17
Qn18
Qn19
Qn20
Qn21
Qn22
Qn23
Qn24
Qn25
Qn26
Qn27
Qn28
BLai
BLbi
MEMORY CELL
MEMORY CELL
IA
IB

FIG. 9

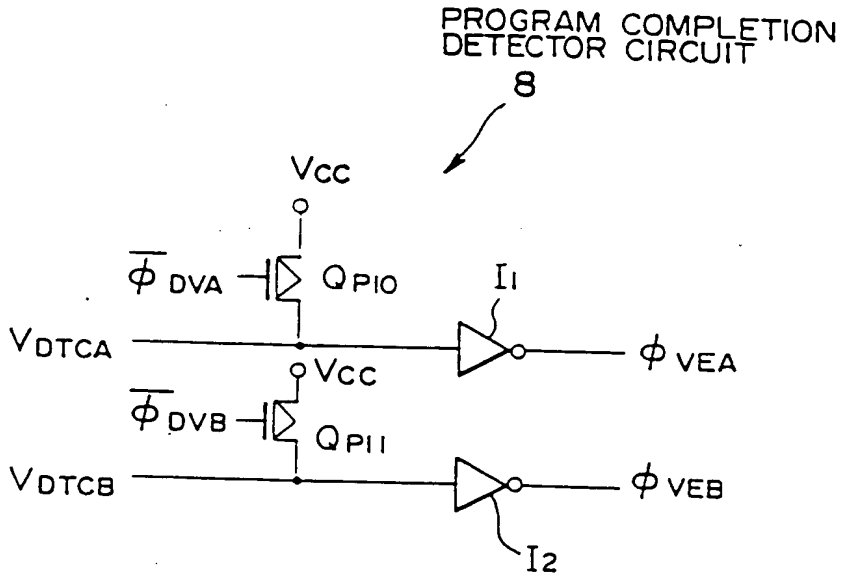

PROGRAM COMPLETION
DETECTOR CIRCUIT
8
Vcc
$\overline{\phi}$ DVA
QP10
I1
VDTCA
ϕ VEA
Vcc
$\overline{\phi}$ DVB
QP11
VDTCB
ϕ VEB
I2

FIG.10

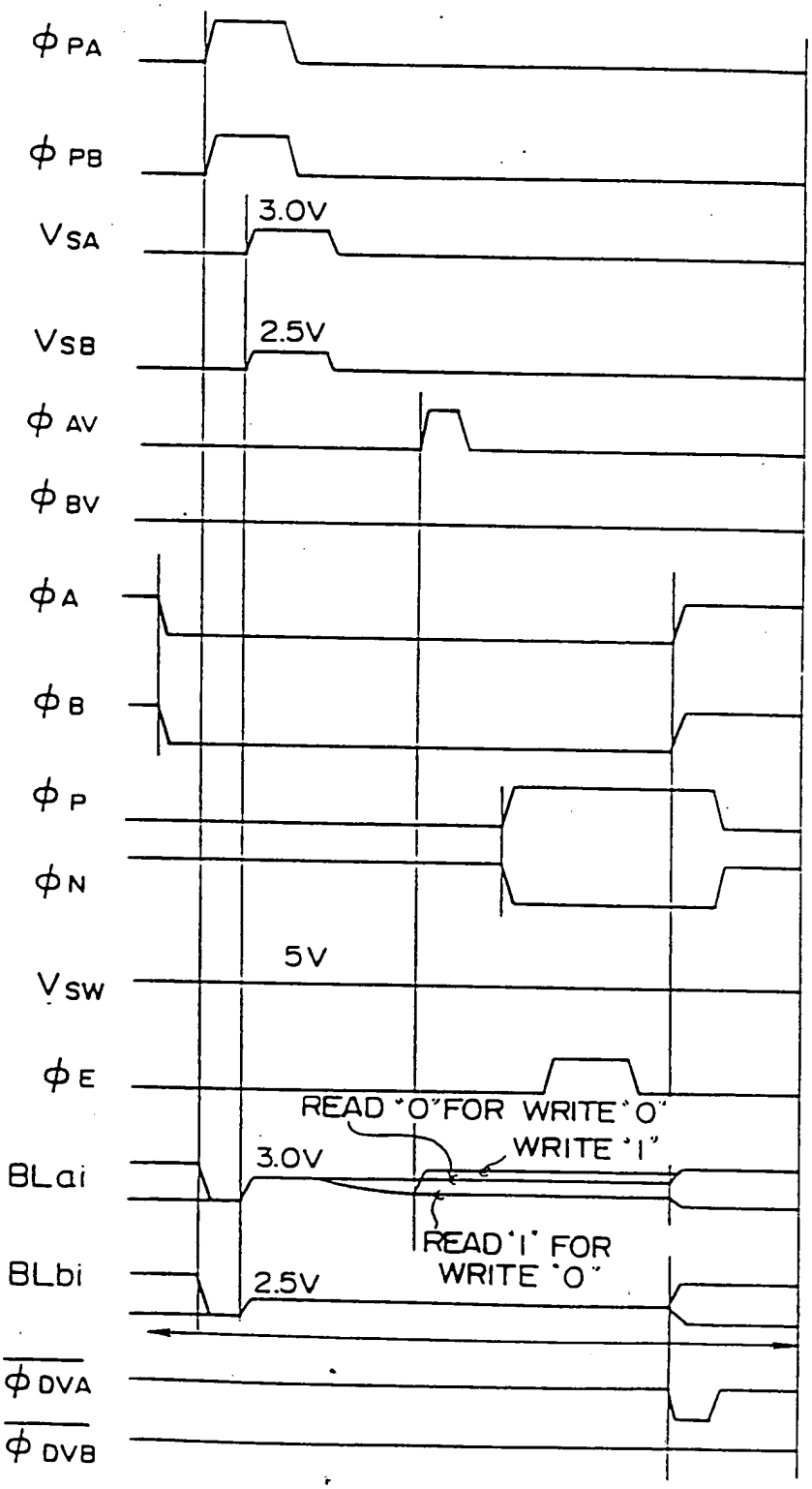

φ PA
φ PB
VSA
3.0V
VSB
2.5V
φ AV
φ BV
φA
φB
φP
φN
VSW
5V
φE
READ "0" FOR WRITE "0"
WRITE "1"
BLai
3.0V
READ "1" FOR WRITE "0"
BLbi
2.5V
φ DVA
φ DVB

FIG.11

FIG. 12(a)

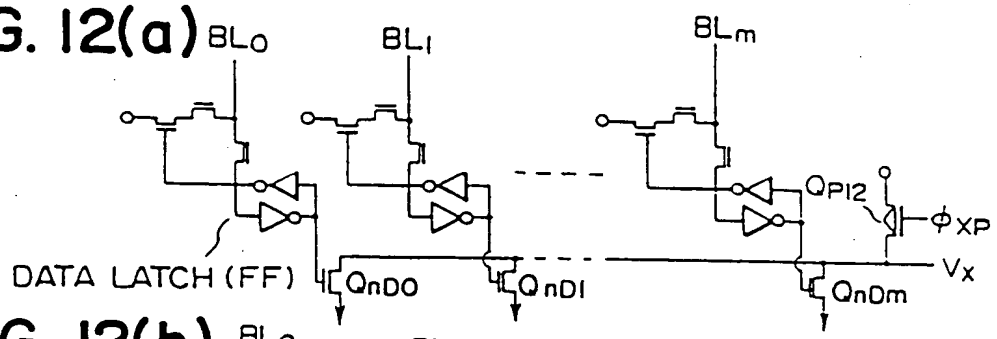


FIG. 12(b)

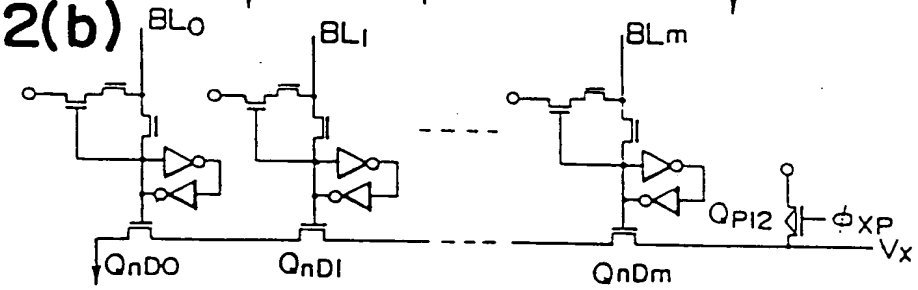


FIG. 12(c)

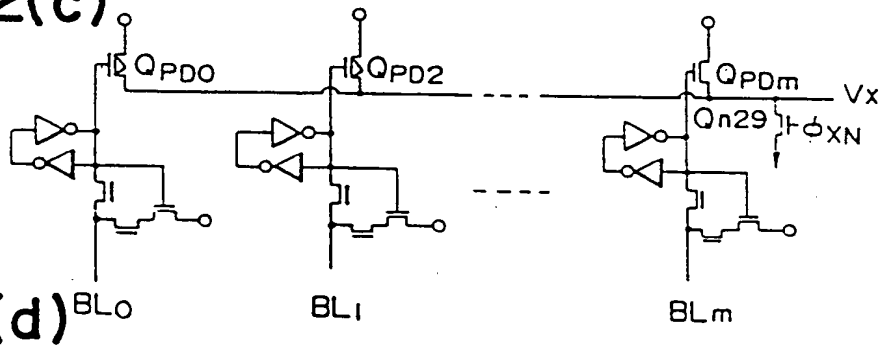


FIG. 12(d)

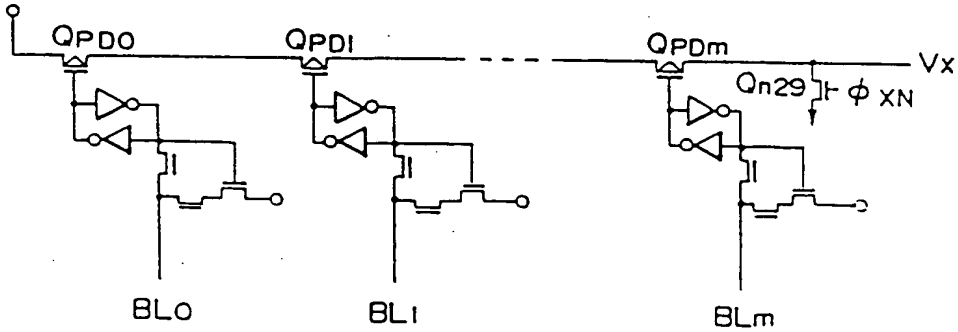


FIG. 13(a)

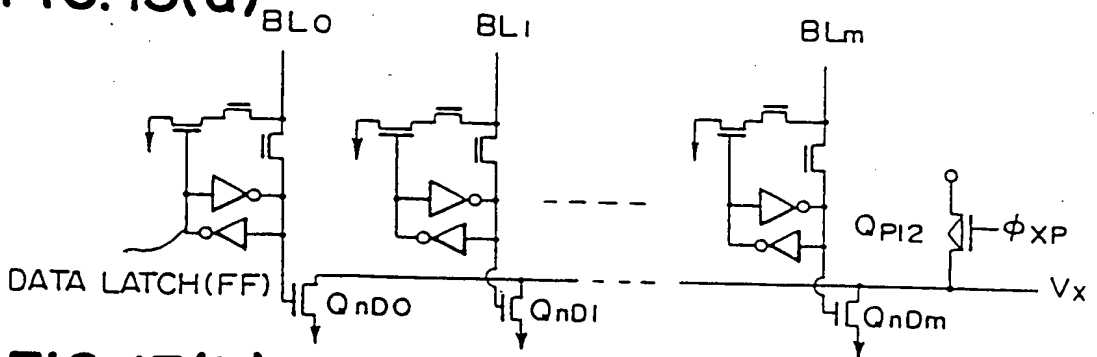


FIG. 13(b)

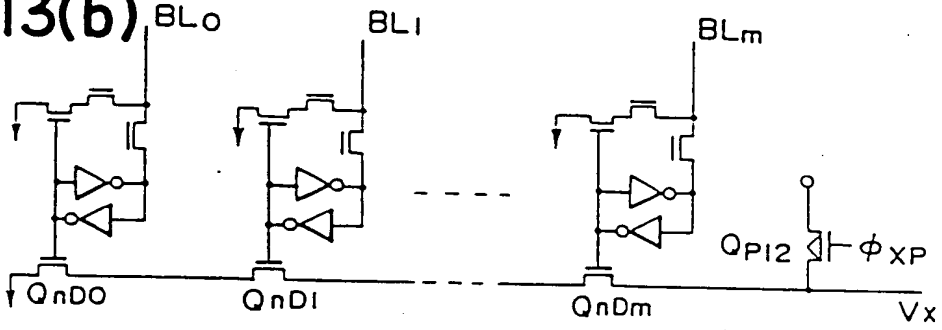


FIG. 13(c)

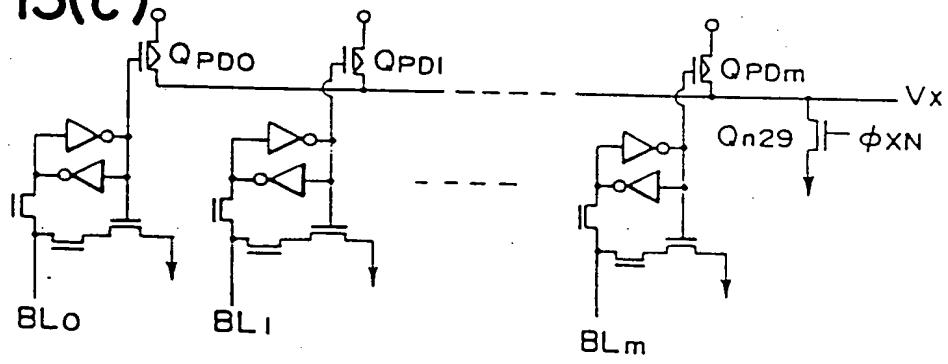
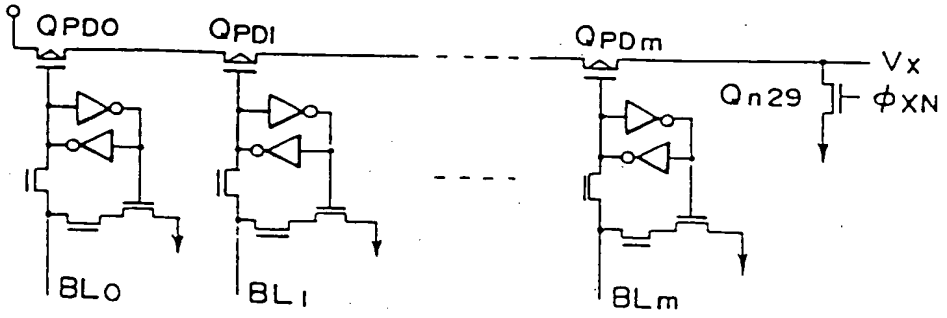


FIG. 13(d)



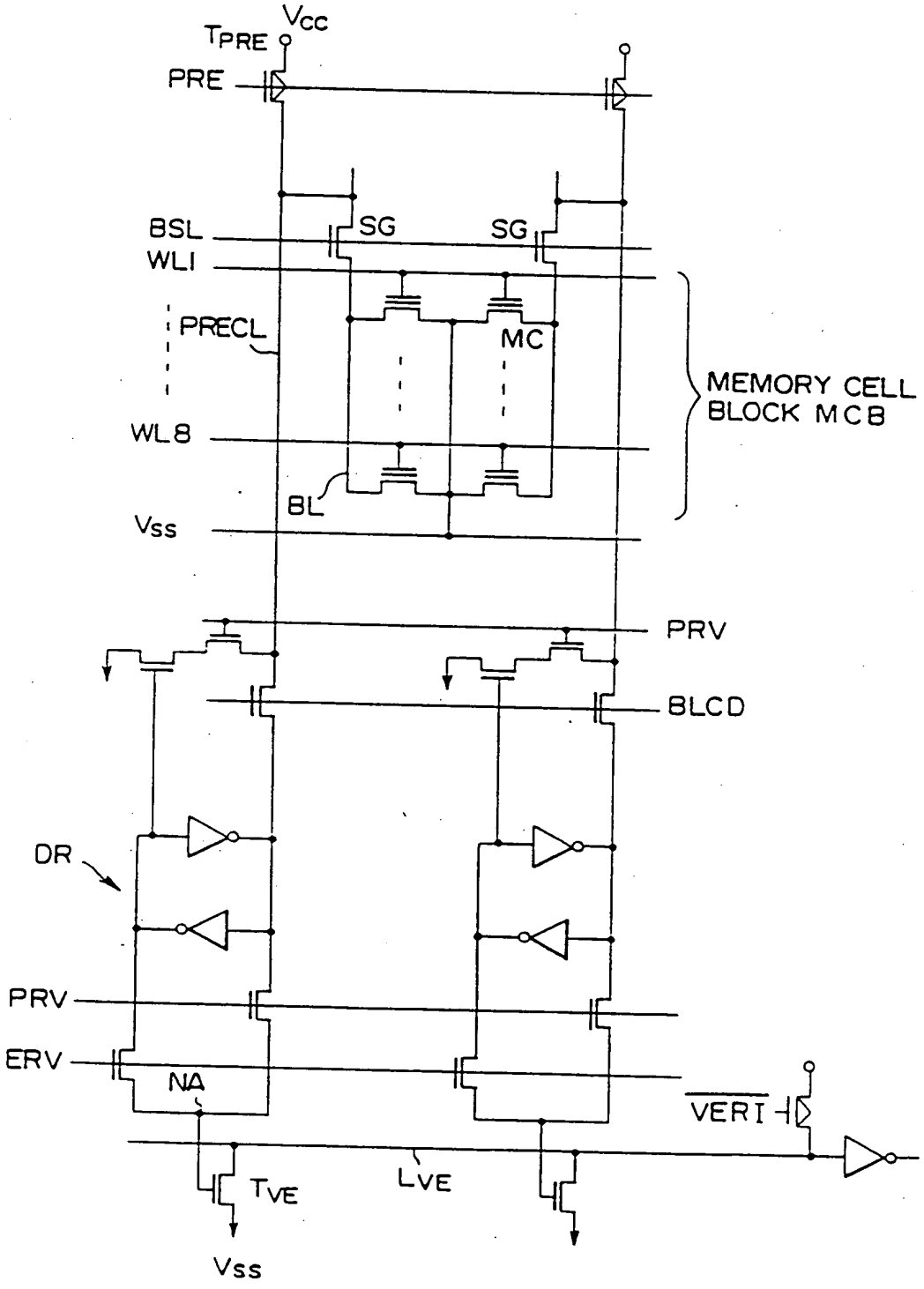

Vcc
TPRE
PRE
BSL
SG
SG
WLI
PRECL
MC
MEMORY CELL
BLOCK MCB
WL8
BL
Vss
PRV
BLCD
DR
PRV
ERV
NA
VERI
TVE
LVE
Vss

FIG. 14

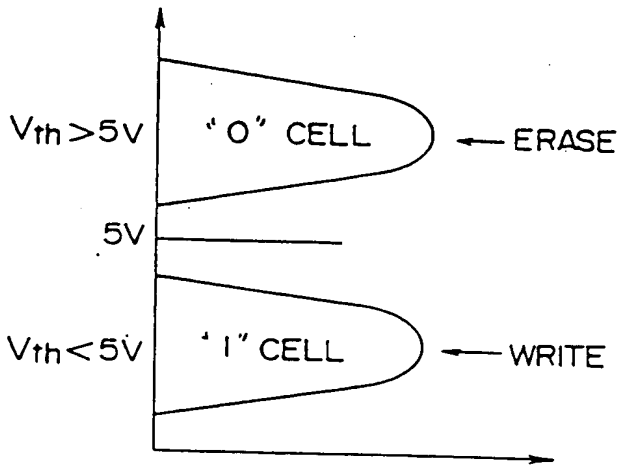


FIG. 15

FIG. 16(a)

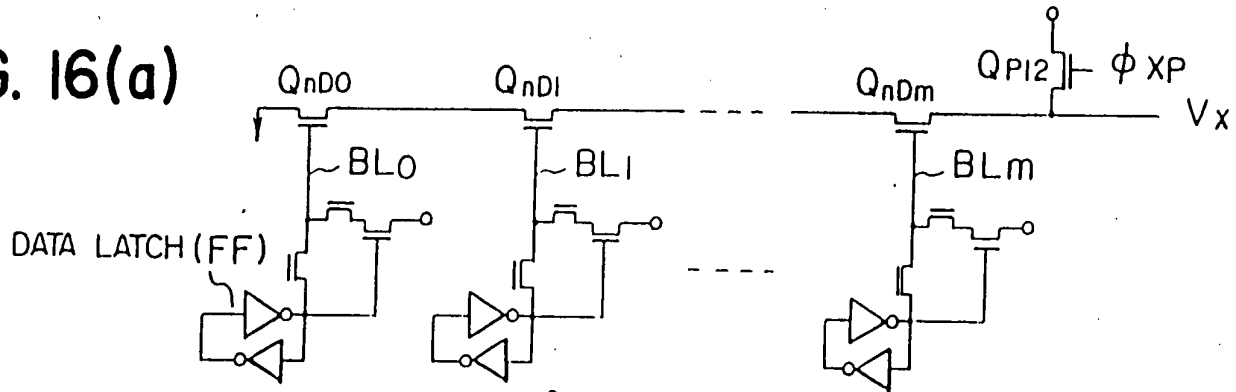


FIG. 16(b)

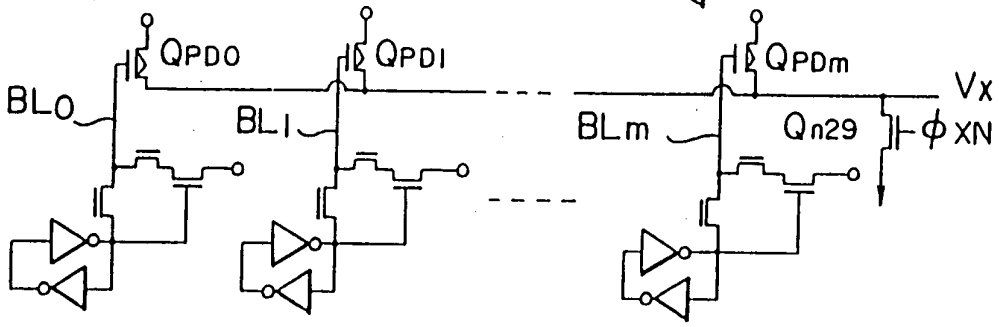


FIG. 17(a)

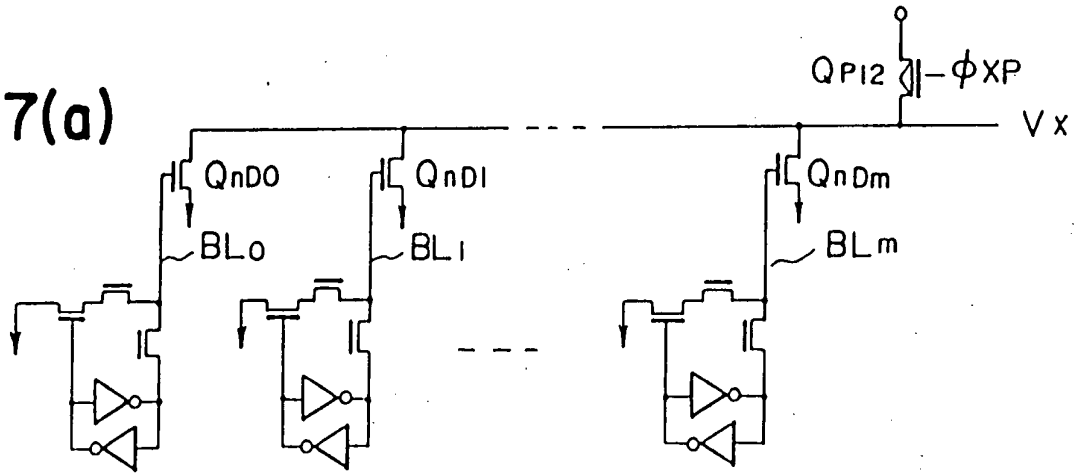


FIG. 17(b)

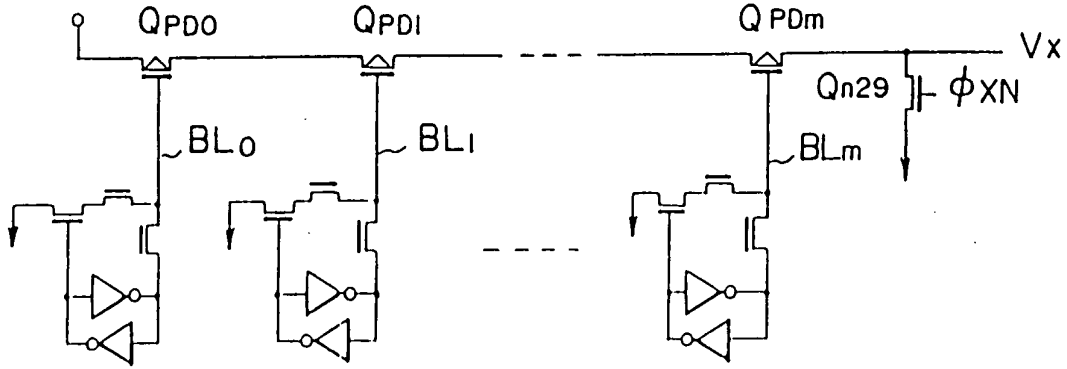


FIG. 18(a)

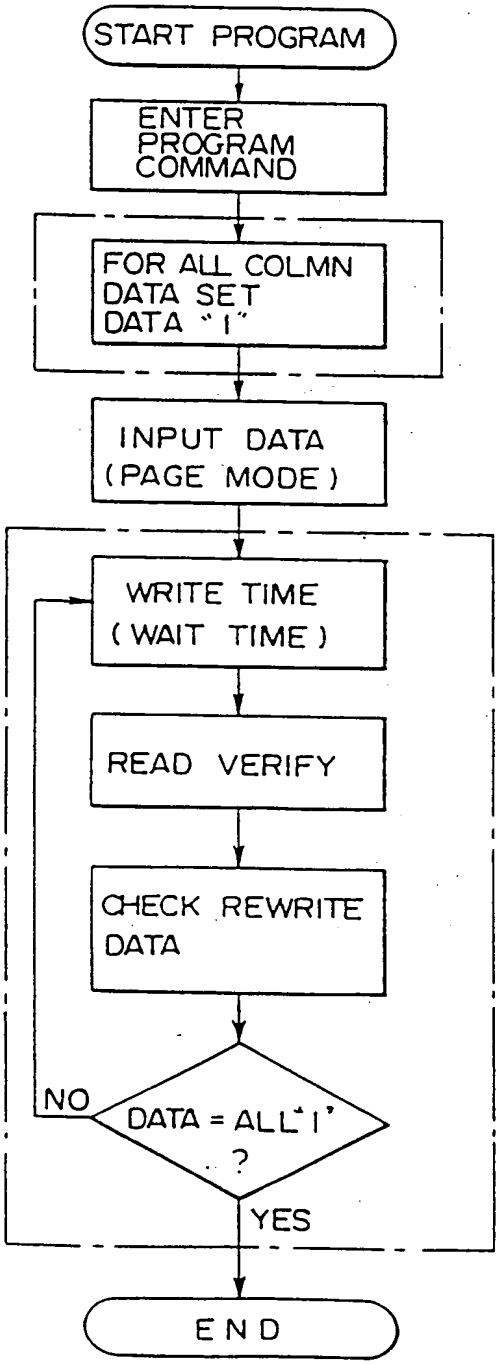


FIG. 18(b)

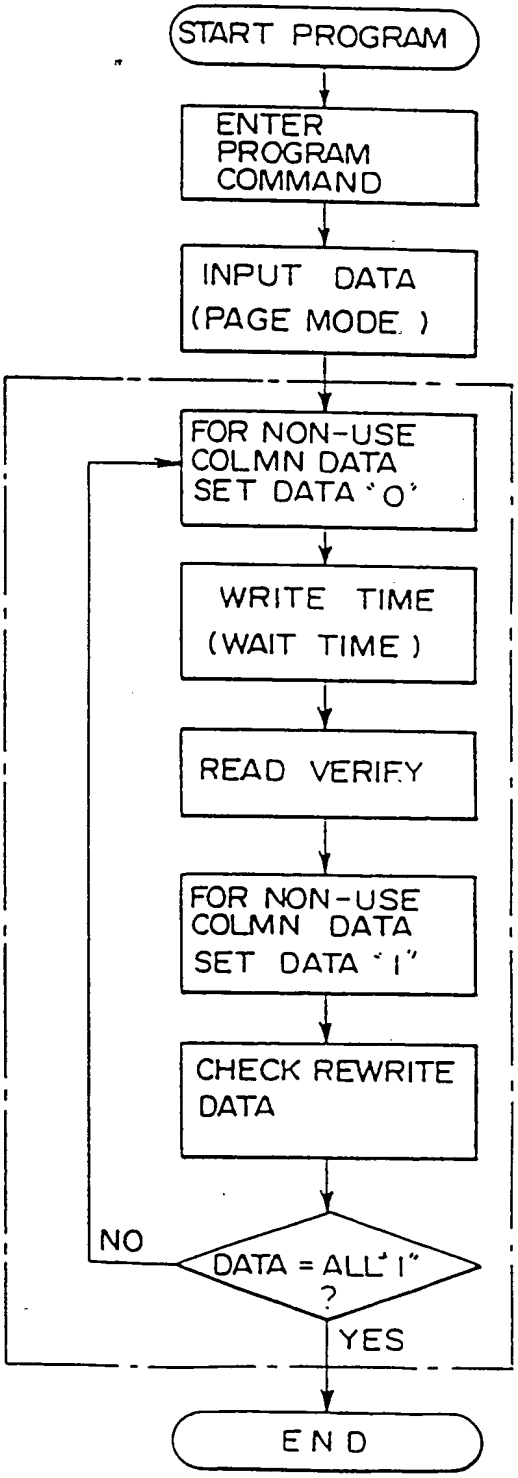


FIG. 19(a)

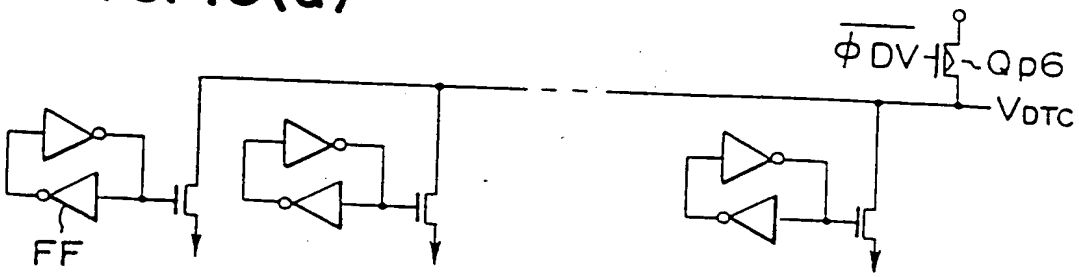


FIG. 19(b)

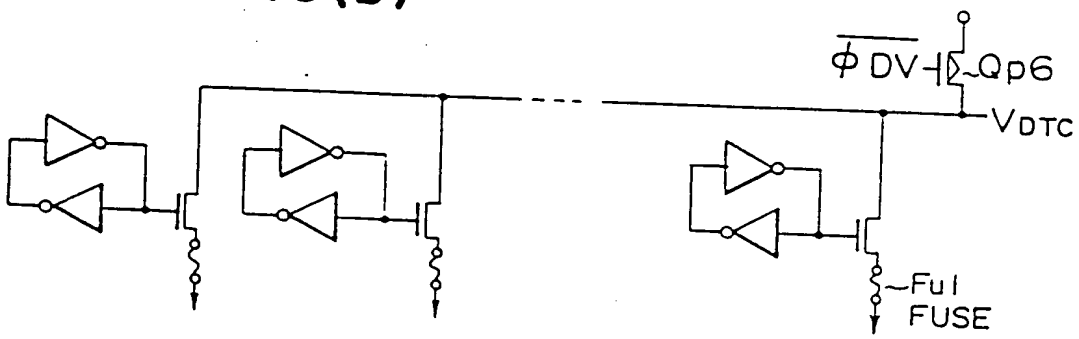


FIG. 19(c)

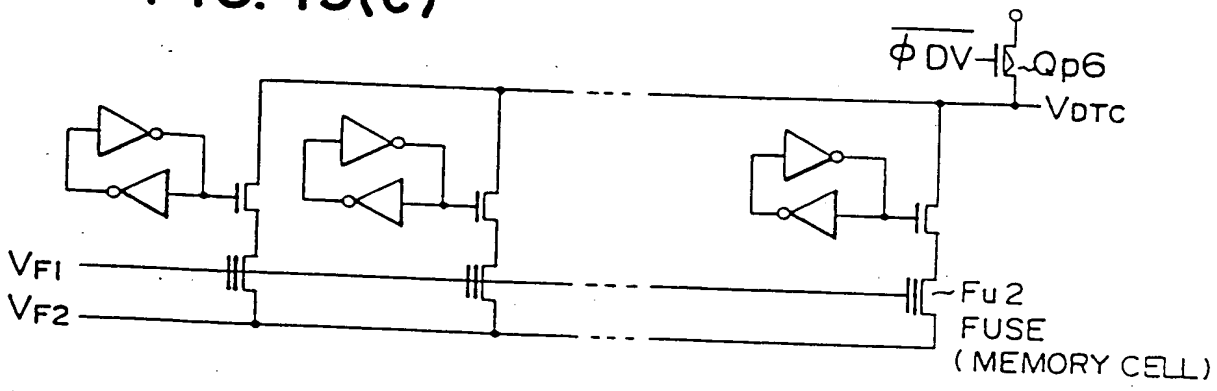


FIG. 20(a)

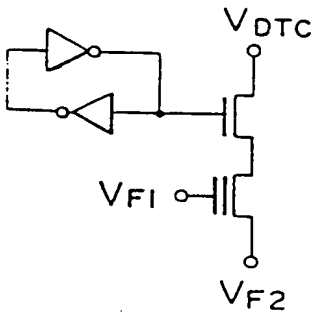


FIG. 20(b)

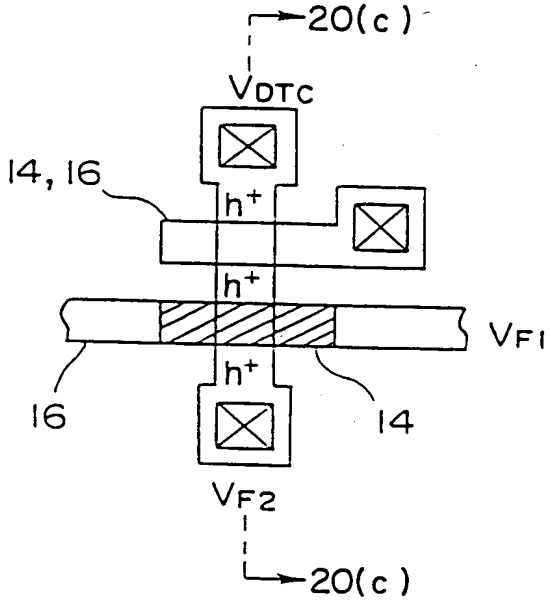


FIG. 20(c)

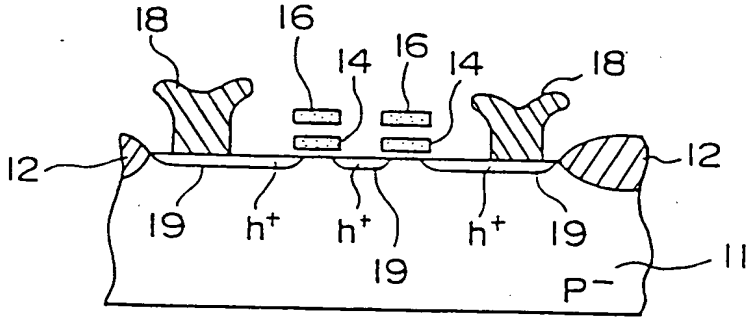


FIG. 21(a)

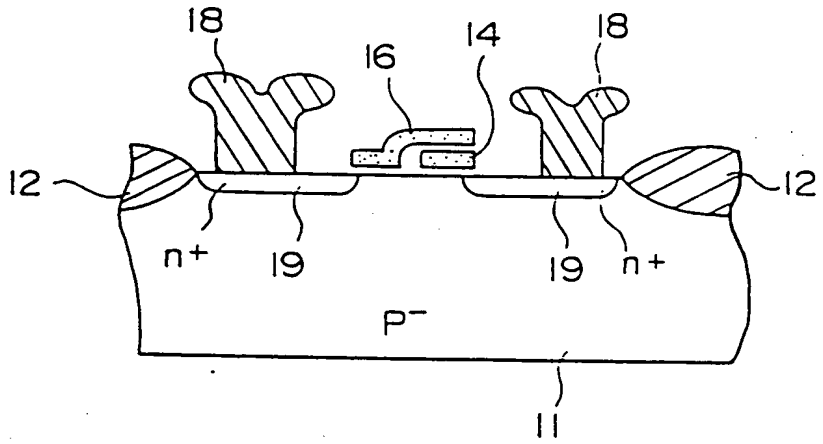


FIG. 21(b)

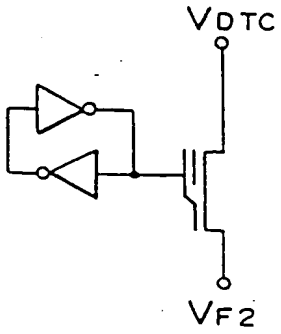
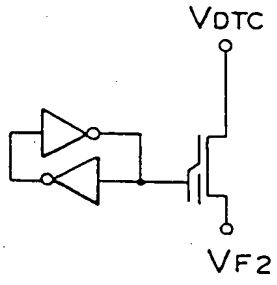


FIG. 21(c)



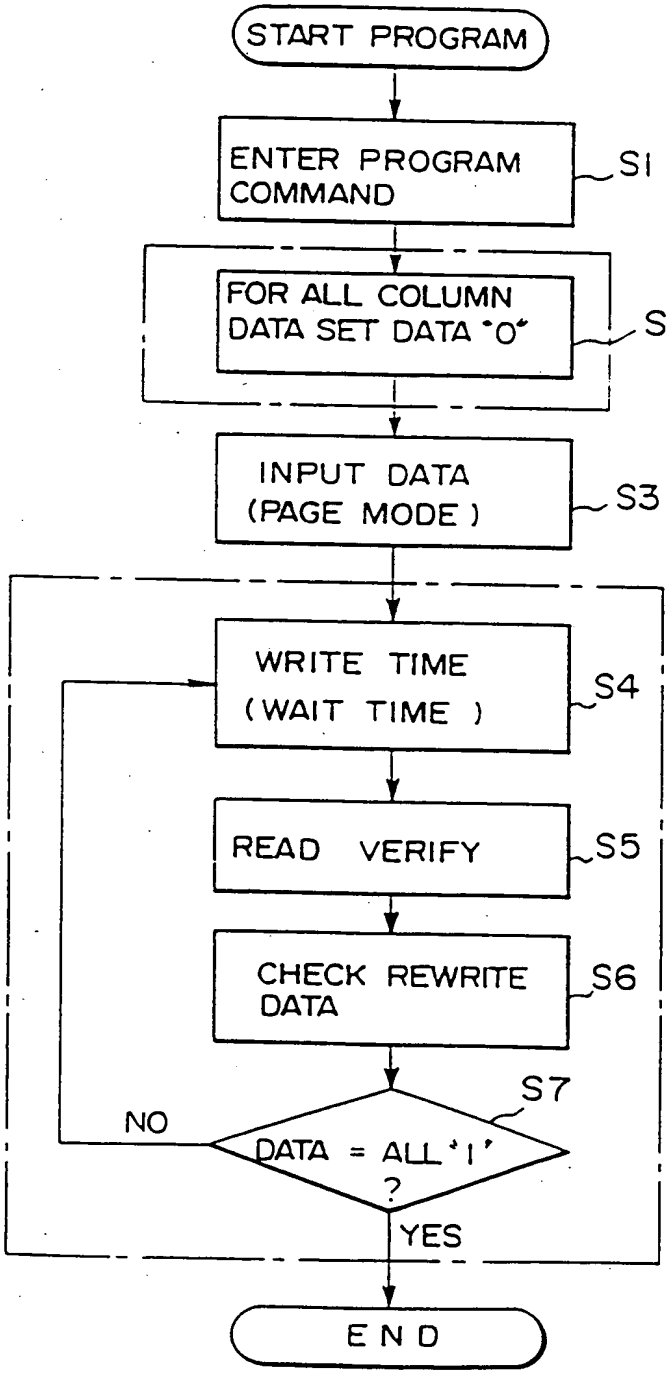

START PROGRAM
ENTER PROGRAM COMMAND
S1
FOR ALL COLUMN DATA SET DATA "0"
S2
INPUT DATA (PAGE MODE)
S3
WRITE TIME (WAIT TIME)
S4
READ VERIFY
S5
CHECK REWRITE DATA
S6
S7
NO
DATA = ALL "1" ?
YES
END

FIG. 22

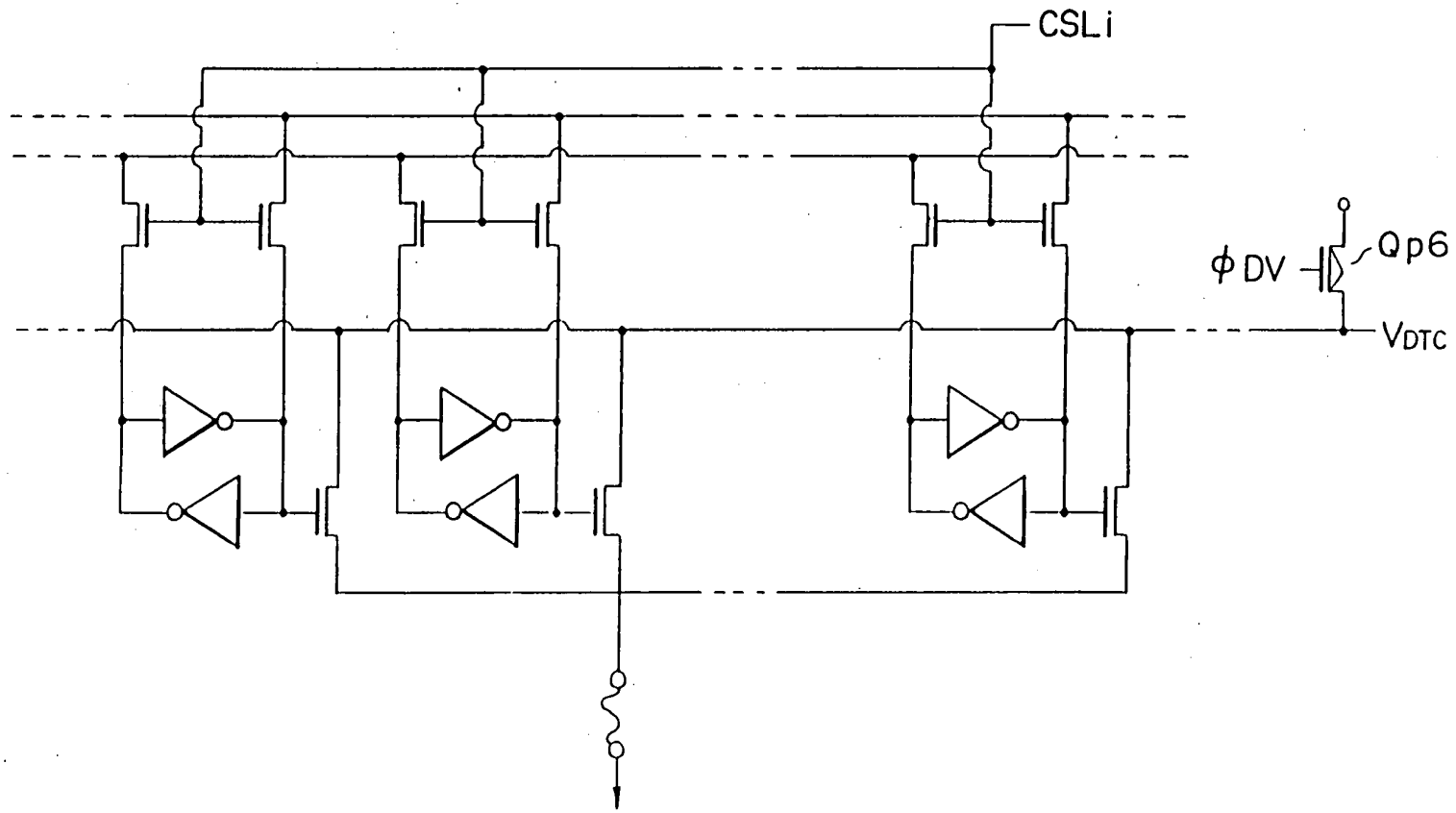


FIG. 23

FIG. 24(a)

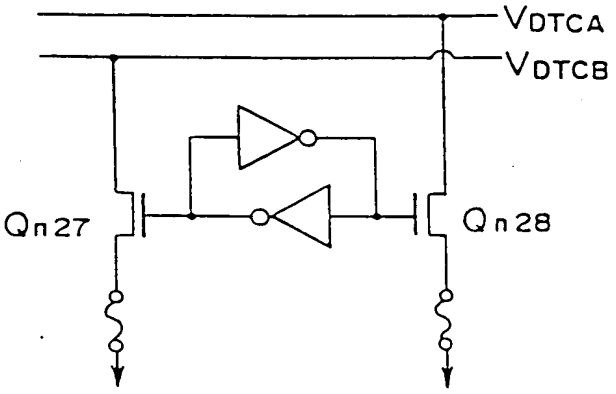


FIG. 24(b)

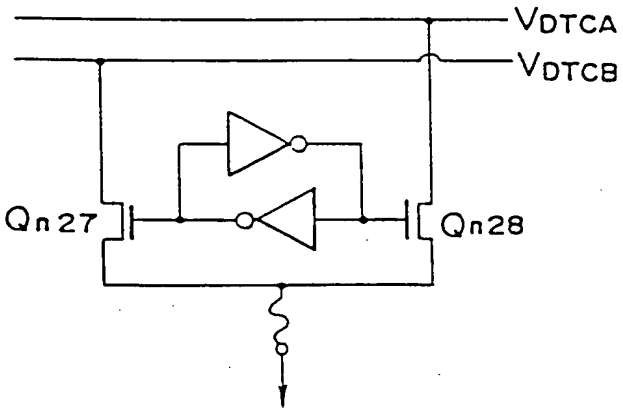


FIG. 25(a)

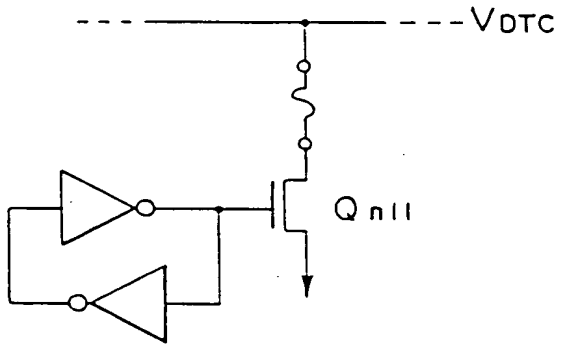


FIG. 25(b)

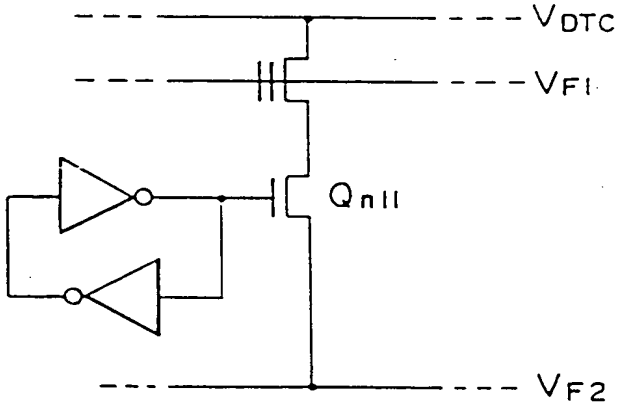


FIG. 26(a)

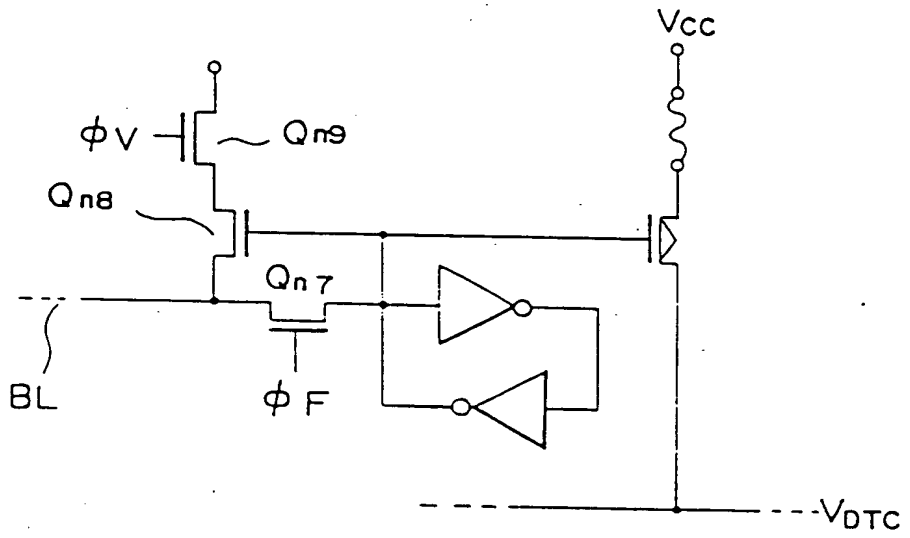


FIG. 26(b)

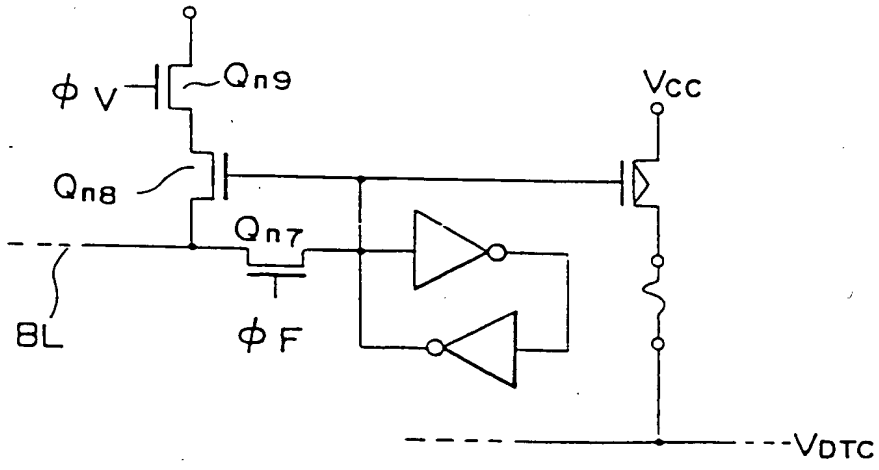


FIG. 27(a)

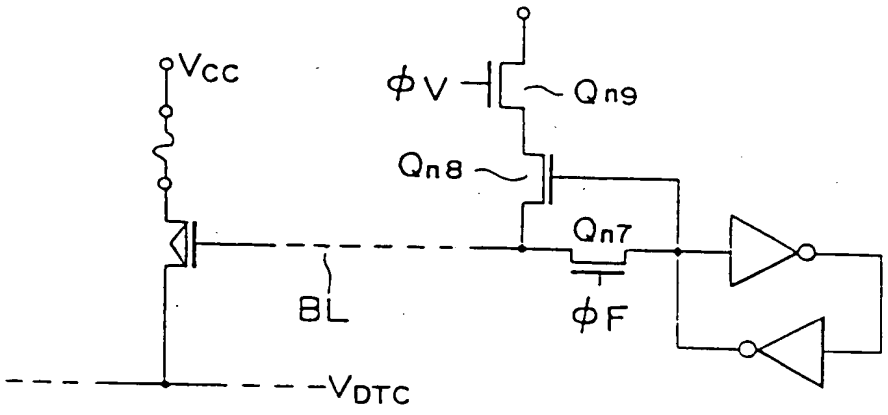


FIG. 27(b)

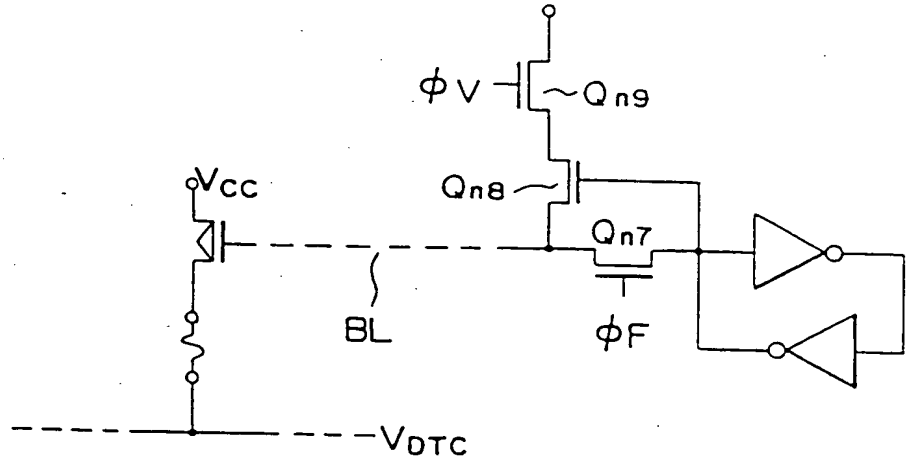


FIG. 28(a)

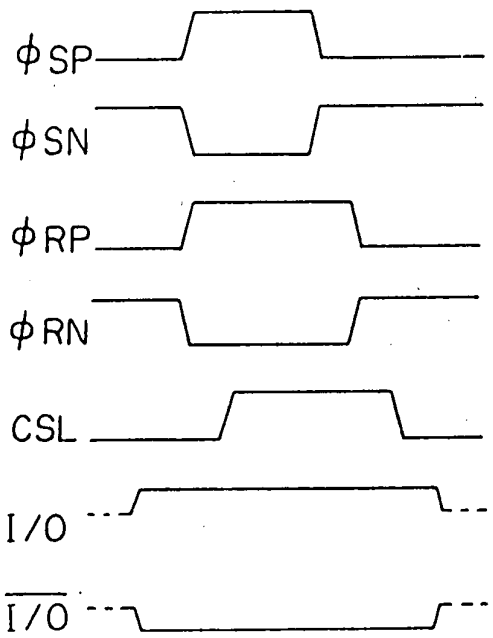
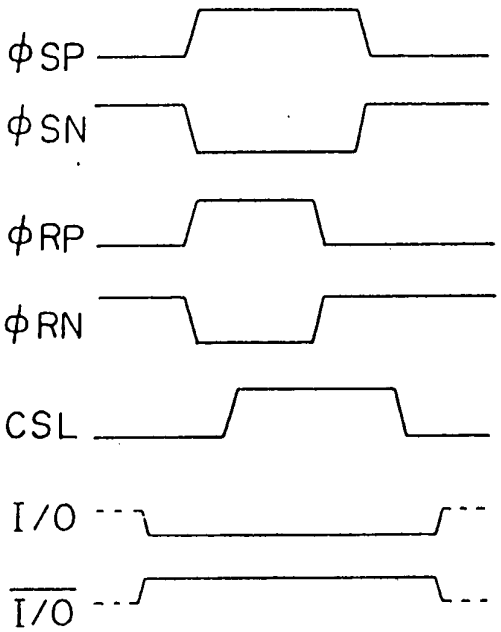


FIG. 28(b)



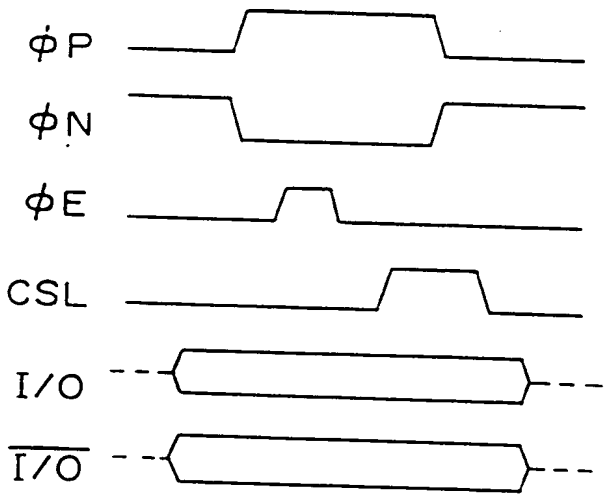


FIG. 29

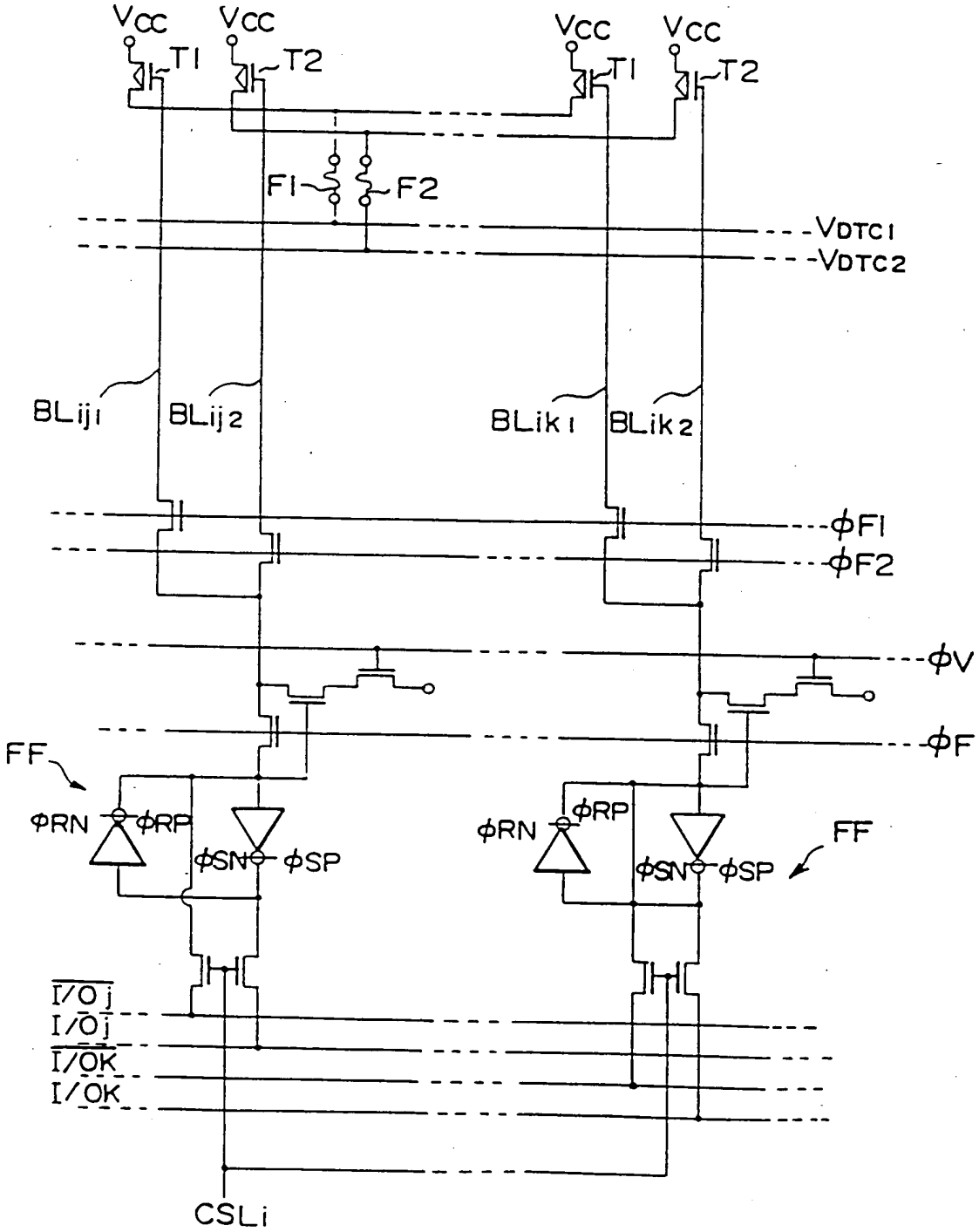

Vcc
Vcc
Vcc
Vcc
T1
T2
T1
T2
F1
F2
VDTC1
VDTC2
BLiji
BLij2
BLik1
BLik2
φF1
φF2
φV
φF
FF
φRN
φRP
φSN
φSP
φRN
φRP
φSN
φSP
FF
I/Oj
I/Oj
I/OK
I/OK
CSLi

FIG. 30

FIG. 31(a)

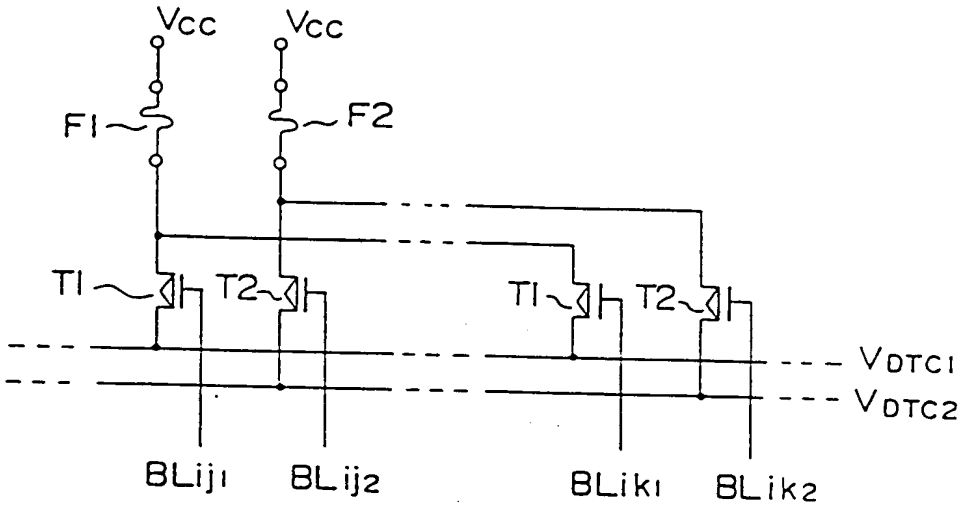
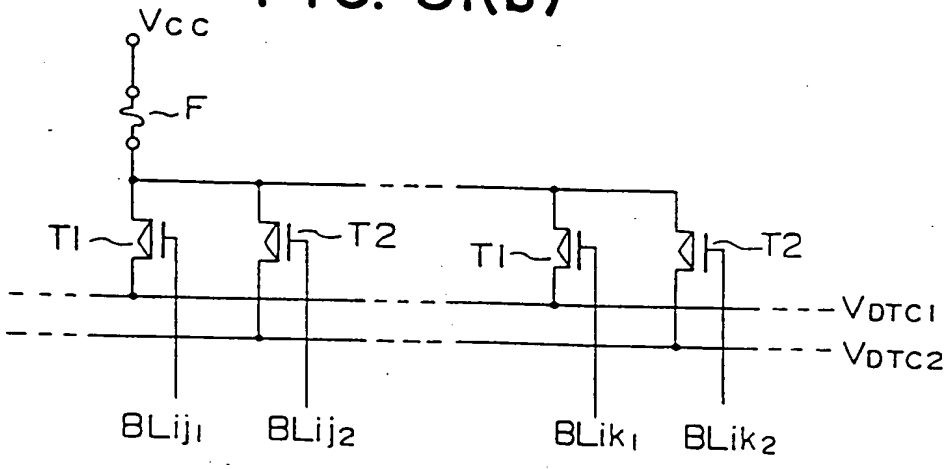


FIG. 31(b)



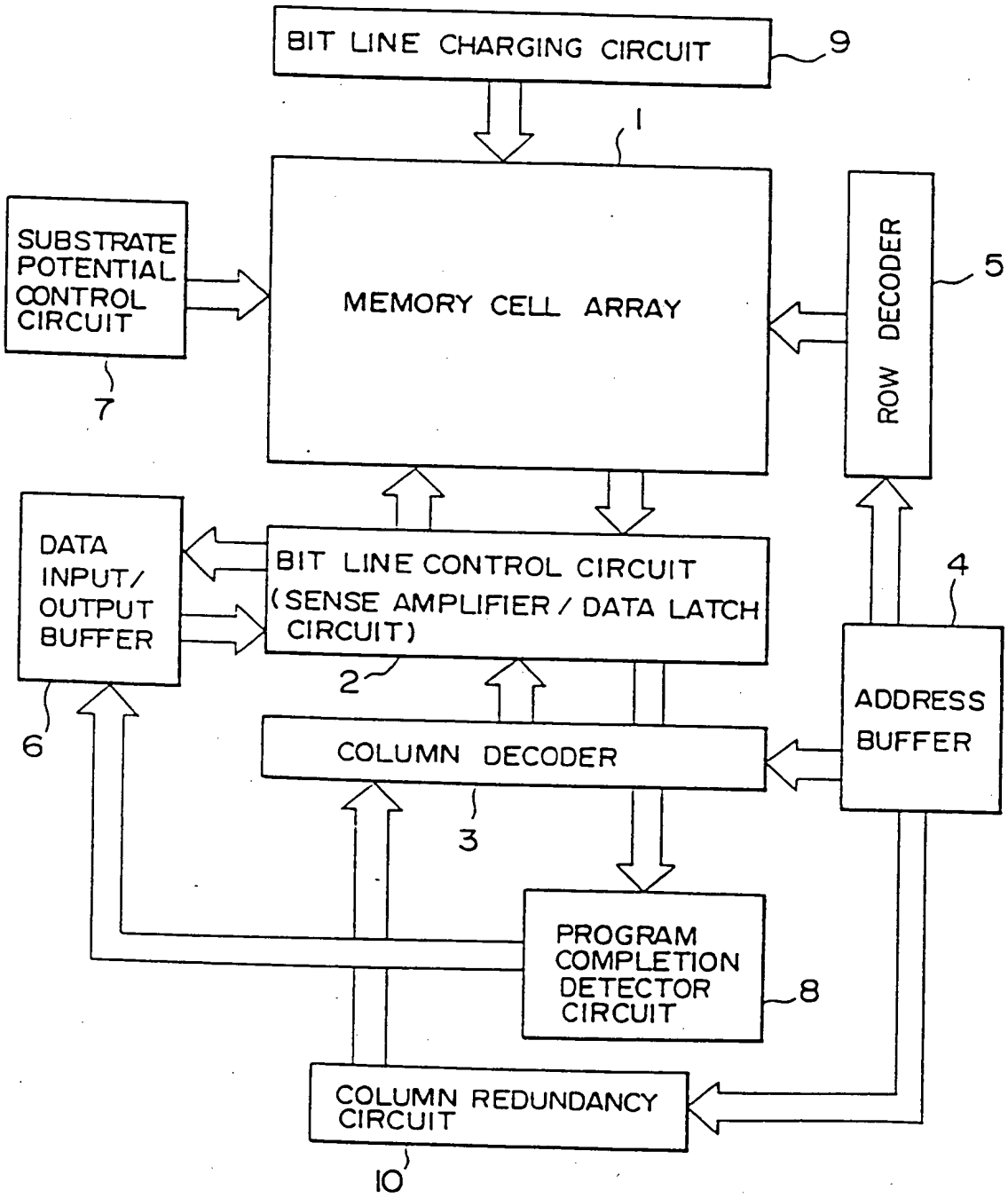

BIT LINE CHARGING CIRCUIT
9
1
SUBSTRATE POTENTIAL CONTROL CIRCUIT
7
MEMORY CELL ARRAY
ROW DECODER
5
DATA INPUT/ OUTPUT BUFFER
6
BIT LINE CONTROL CIRCUIT (SENSE AMPLIFIER / DATA LATCH CIRCUIT)
2
4
ADDRESS BUFFER
COLUMN DECODER
3
PROGRAM COMPLETION DETECTOR CIRCUIT
8
COLUMN REDUNDANCY CIRCUIT
10

FIG. 32

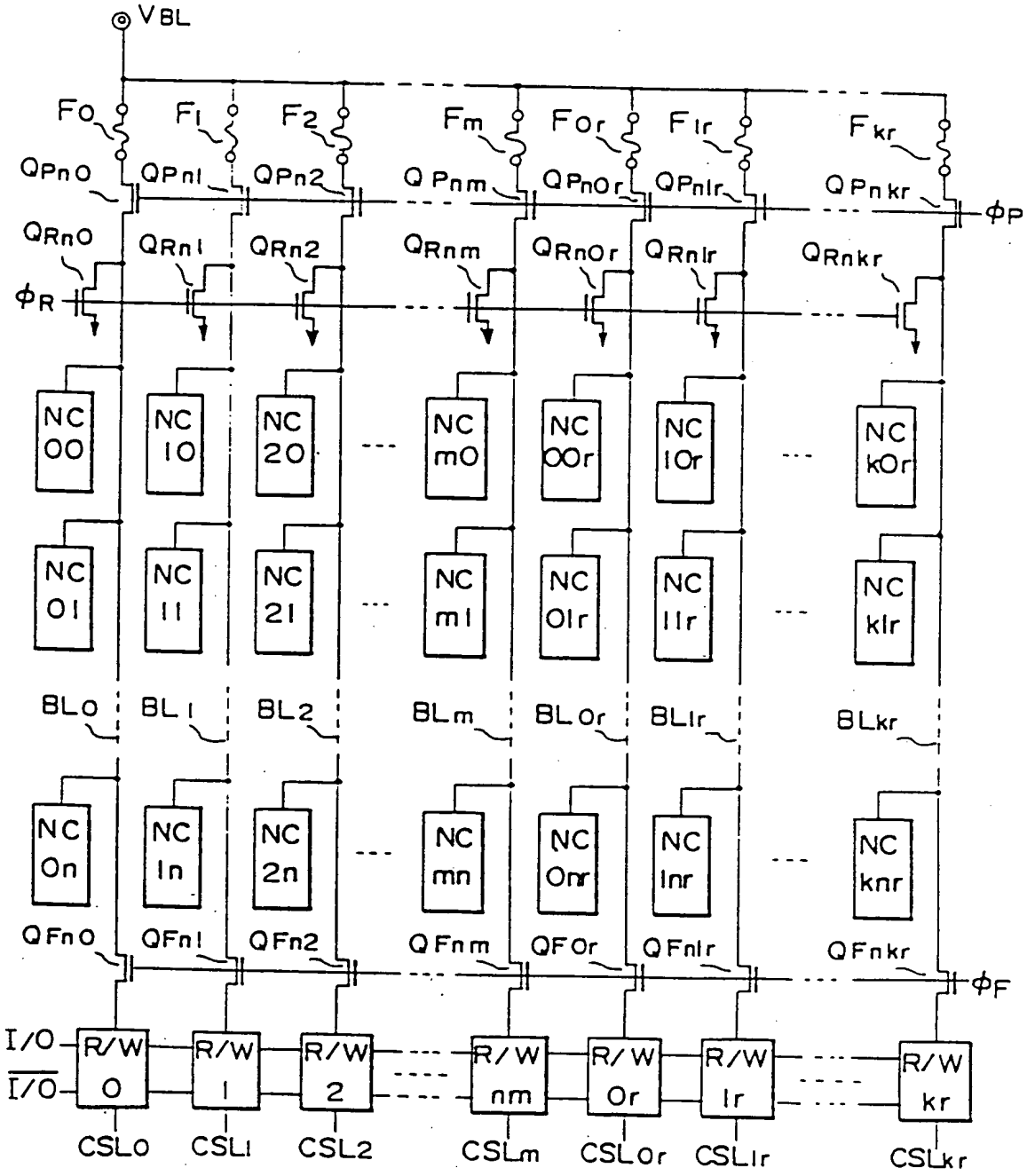

VBL
F0
F1
F2
Fm
For
Flr
Fkr
QPn0
QPn1
QPn2
QPnm
QPn0r
QPn1r
QPnkr
φP
QRn0
QRn1
QRn2
QRnm
QRn0r
QRn1r
QRnkr
φR
NC 00
NC 10
NC 20
NC m0
NC 00r
NC 10r
NC k0r
NC 01
NC 11
NC 21
NC m1
NC 01r
NC 11r
NC k1r
BL0
BL1
BL2
BLm
BL0r
BL1r
BLkr
NC 0n
NC 1n
NC 2n
NC mn
NC 0nr
NC 1nr
NC knr
QFn0
QFn1
QFn2
QFnm
QF0r
QFn1r
QFnkr
φF
I/O
I/O
R/W 0
R/W 1
R/W 2
R/W nm
R/W 0r
R/W 1r
R/W kr
CSL0
CSL1
CSL2
CSLm
CSL0r
CSL1r
CSLkr

FIG. 33

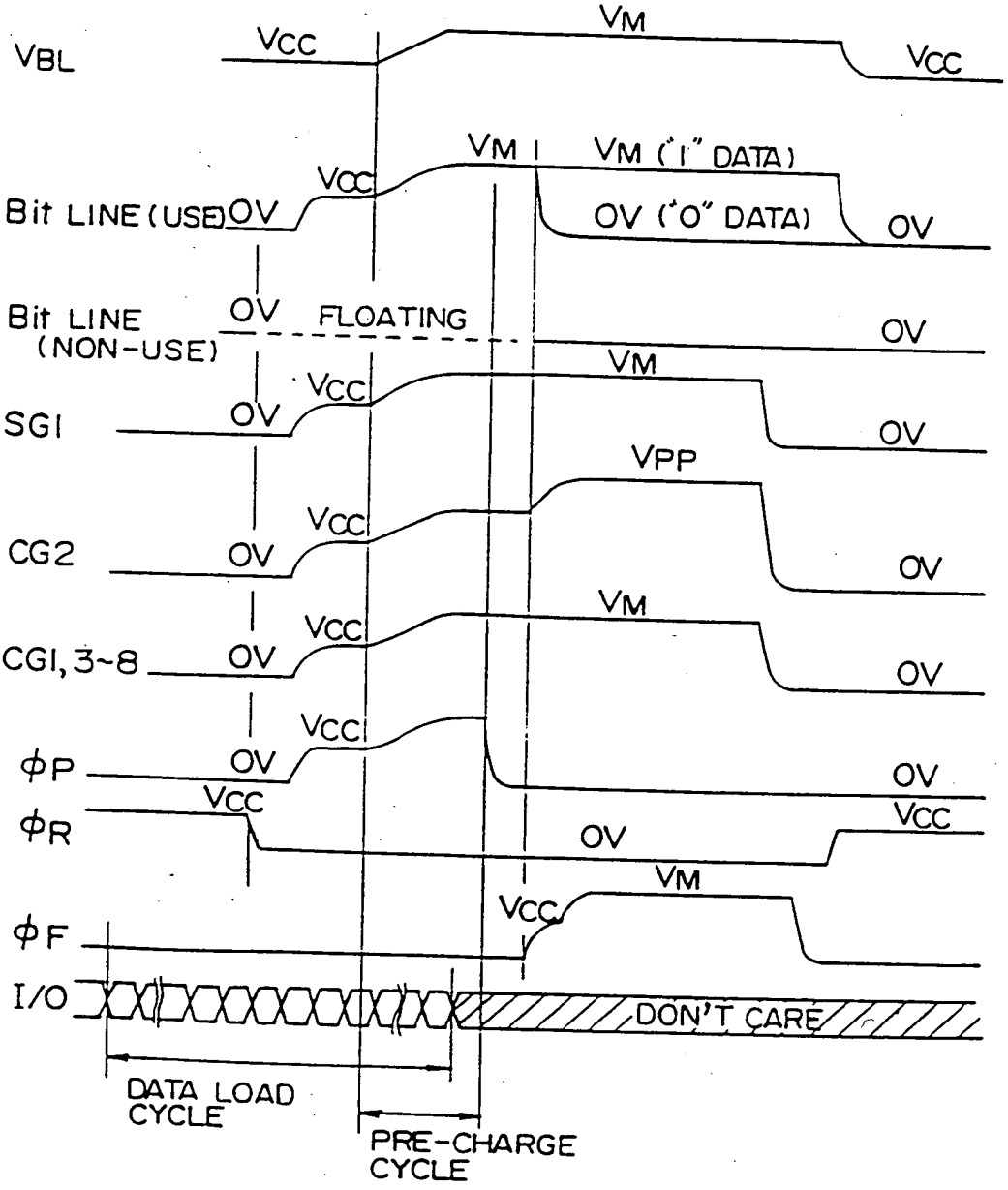

VBL
Vcc
VM
Vcc
Bit LINE (USE)
OV
Vcc
VM
VM ("1" DATA)
OV ("0" DATA)
OV
Bit LINE (NON-USE)
OV
FLOATING
OV
SGI
OV
Vcc
VM
OV
CG2
OV
Vcc
VPP
OV
CGI, 3~8
OV
Vcc
VM
OV
ϕP
OV
Vcc
OV
ϕR
Vcc
OV
Vcc
ϕF
Vcc
VM
I/O
DON'T CARE
DATA LOAD CYCLE
PRE-CHARGE CYCLE

FIG. 34

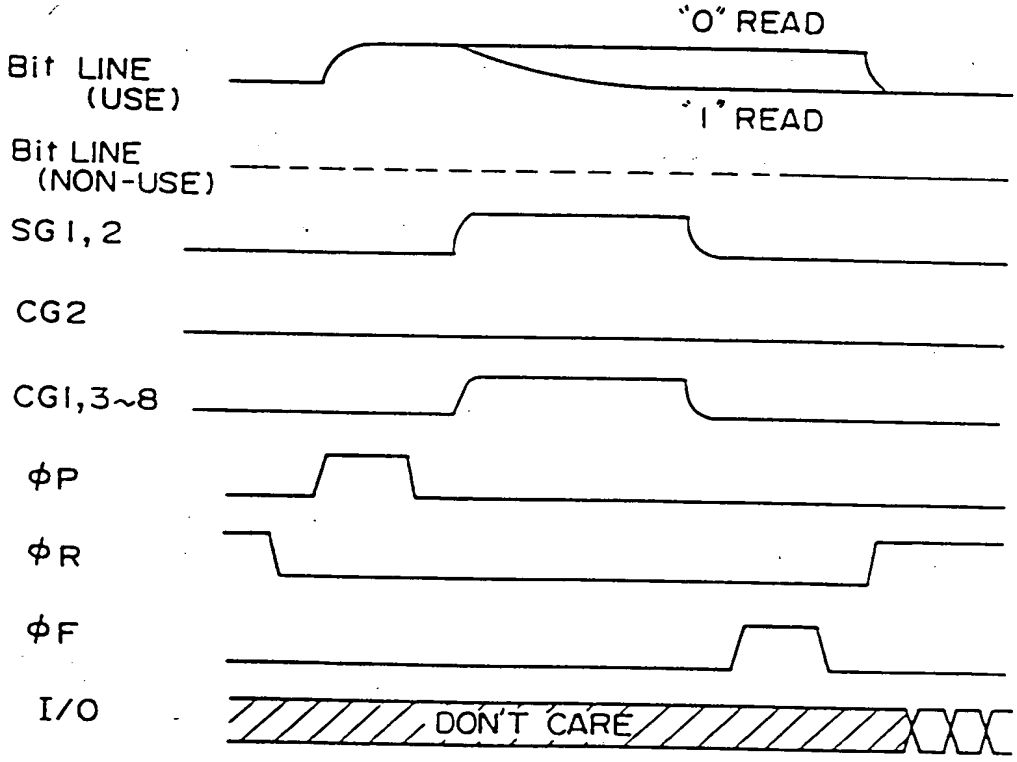

"0" READ
Bit LINE (USE)
"1" READ
Bit LINE (NON-USE)
SG1,2
CG2
CG1,3~8
φP
φR
φF
I/O
DON'T CARE

FIG.35

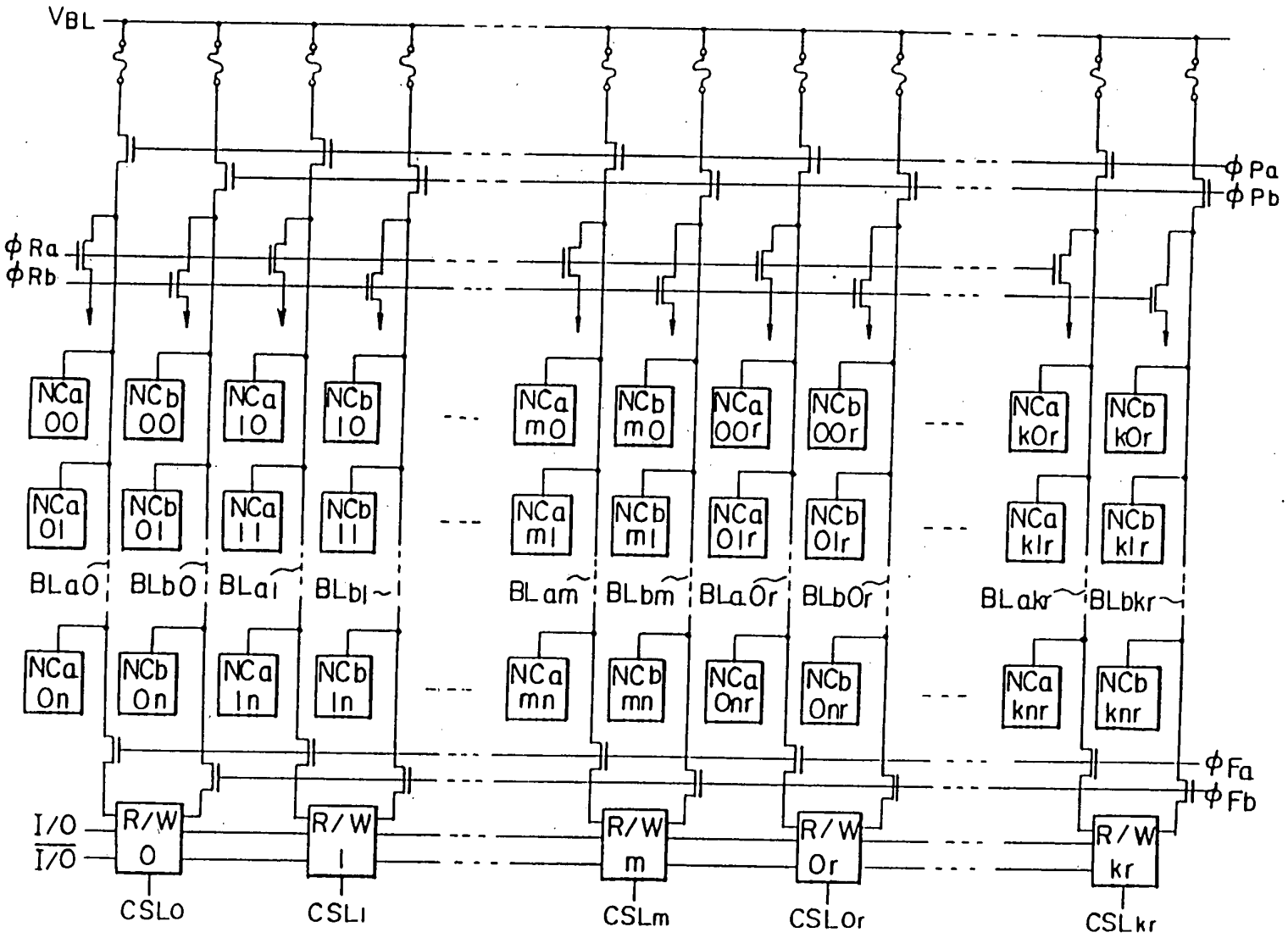

VBL
φRa
φRb
φPa
φPb
NCa 00
NCb 00
NCa 10
NCb 10
NCa m0
NCb m0
NCa 00r
NCb 00r
NCa k0r
NCb k0r
NCa 01
NCb 01
NCa 11
NCb 11
NCa m1
NCb m1
NCa 01r
NCb 01r
NCa k1r
NCb k1r
BLa0
BLb0
BLa1
BLb1
BLam
BLbm
BLa0r
BLb0r
BLakr
BLbkr
NCa 0n
NCb 0n
NCa 1n
NCb 1n
NCa mn
NCb mn
NCa 0nr
NCb 0nr
NCa knr
NCb knr
φFa
φFb
I/O
I/O
R/W 0
R/W 1
R/W m
R/W 0r
R/W kr
CSL0
CSL1
CSLm
CSL0r
CSLkr

FIG.36

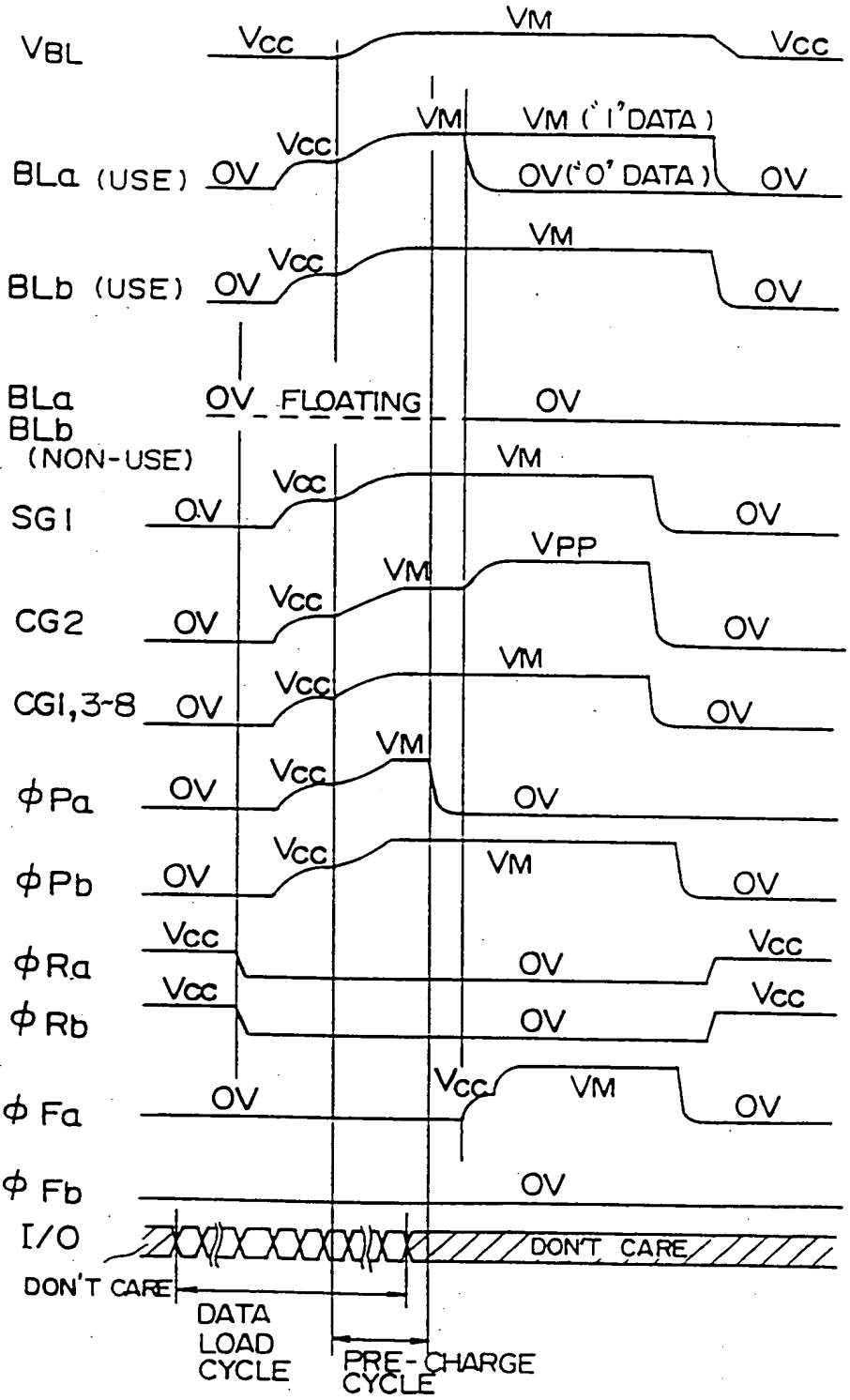

VBL
Vcc
VM
Vcc
BLa (USE)
OV
Vcc
VM
VM ('1' DATA)
OV ('0' DATA)
OV
BLb (USE)
OV
Vcc
VM
OV
BLa
BLb
(NON-USE)
OV
FLOATING
OV
SG1
OV
Vcc
VM
OV
CG2
OV
Vcc
VM
VPP
OV
CG1,3-8
OV
Vcc
VM
OV
φPa
OV
Vcc
VM
OV
φPb
OV
Vcc
VM
OV
φRa
Vcc
OV
Vcc
φRb
Vcc
OV
Vcc
φFa
OV
Vcc
VM
OV
φFb
OV
I/O
DON'T CARE
DON'T CARE
DATA LOAD CYCLE
PRE-CHARGE CYCLE

FIG. 37

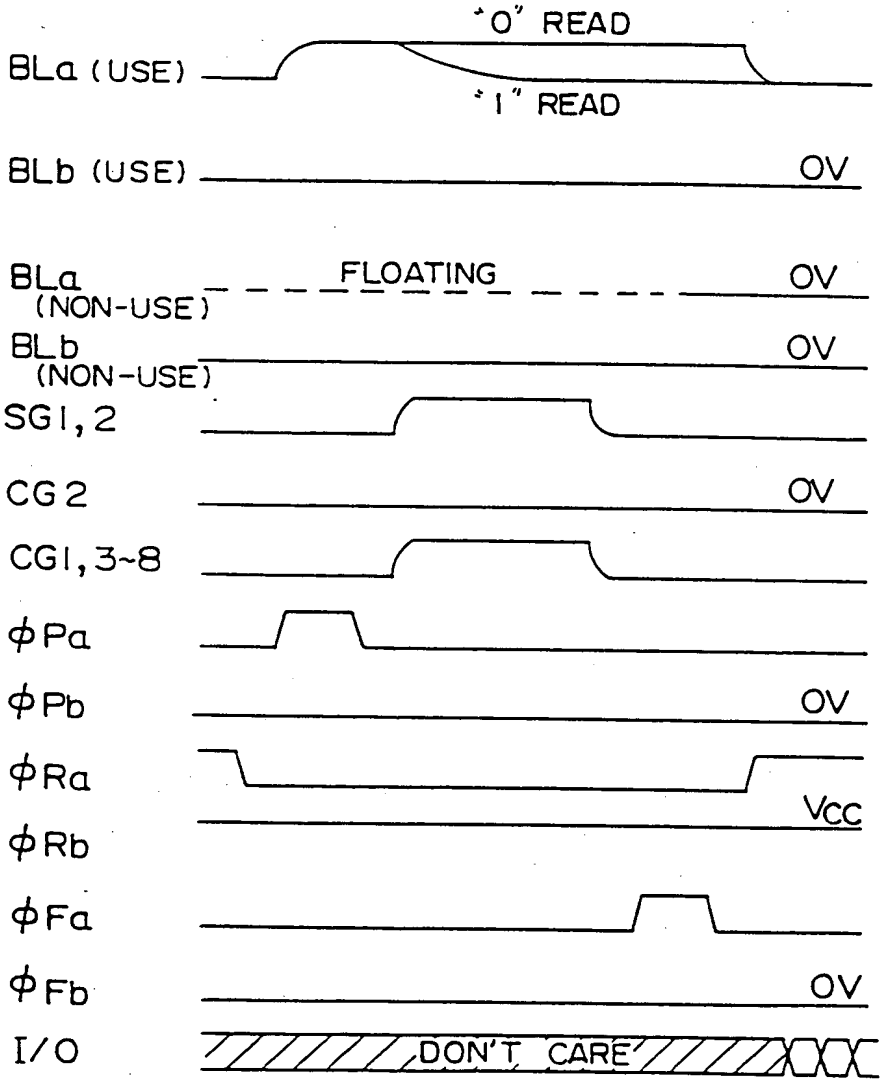

"0" READ
BLa (USE)
"1" READ
BLb (USE)
OV
BLa (NON-USE)
FLOATING
OV
BLb (NON-USE)
OV
SG1, 2
CG2
OV
CG1, 3~8
φPa
φPb
OV
φRa
Vcc
φRb
φFa
φFb
OV
I/O
DON'T CARE

FIG. 38

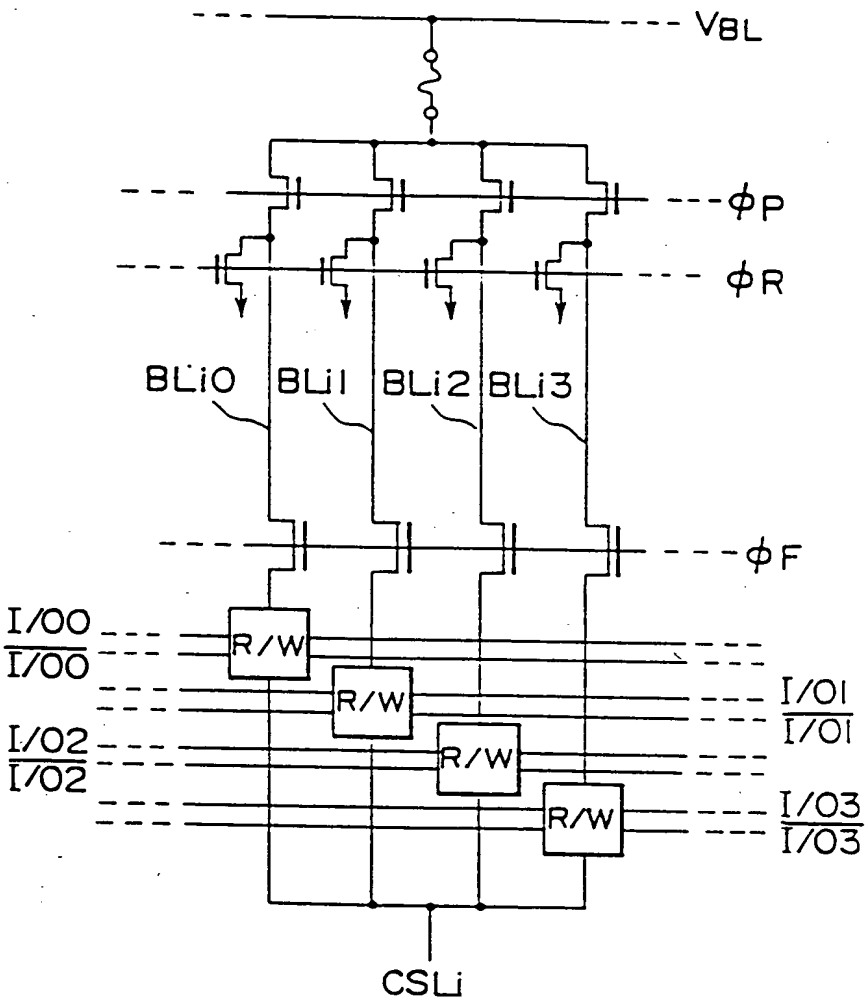

VBL
φP
φR
BLi0
BLi1
BLi2
BLi3
φF
I/00
I/00
R/W
R/W
R/W
R/W
I/01
I/01
I/02
I/02
I/03
I/03
CSLi

FIG.39

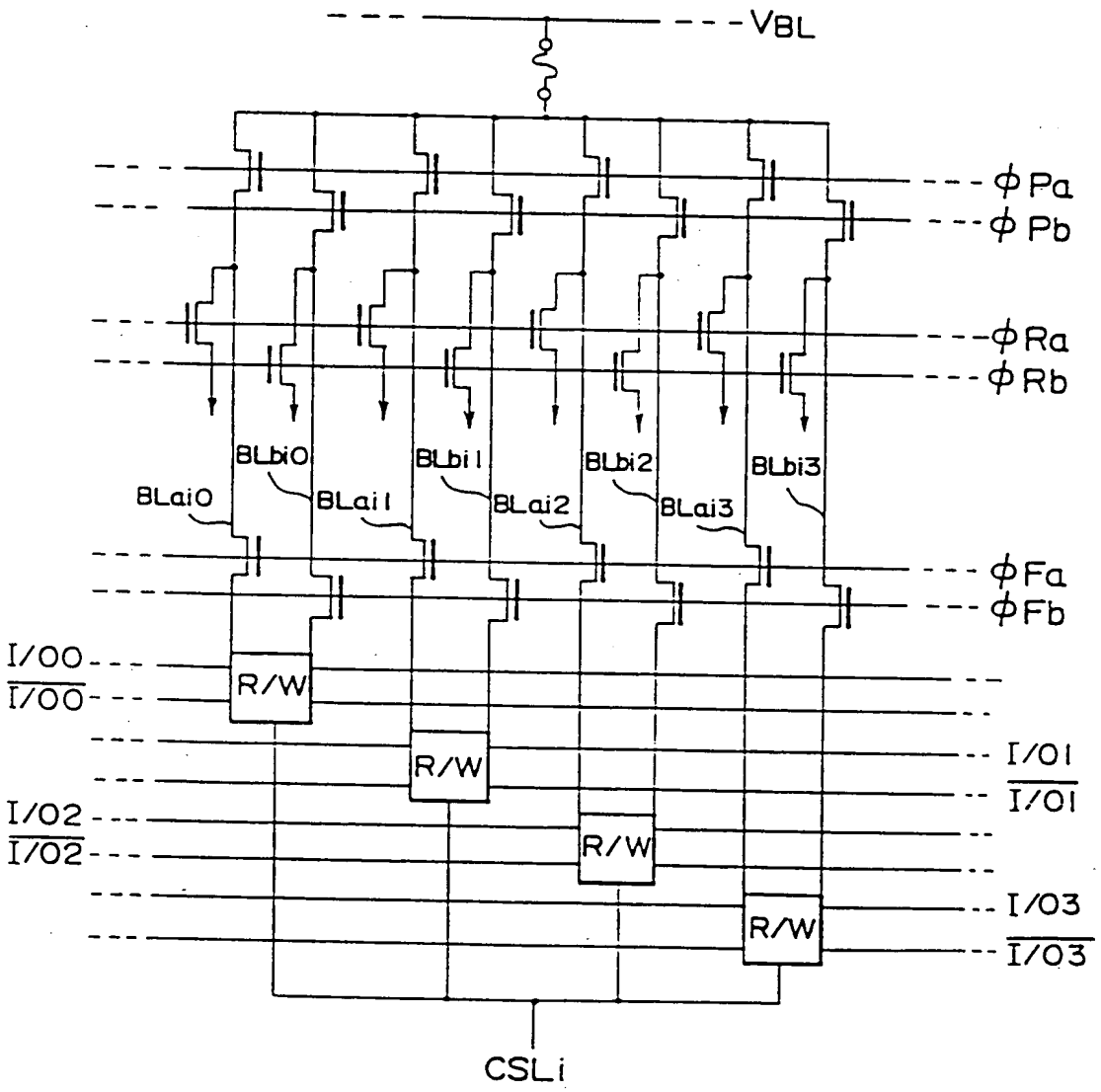

VBL
φPa
φPb
φRa
φRb
BLbi0
BLbi1
BLbi2
BLbi3
BLai0
BLai1
BLai2
BLai3
φFa
φFb
I/00
I/00
R/W
R/W
R/W
R/W
I/01
I/01
I/02
I/02
I/03
I/03
CSLi

FIG. 40

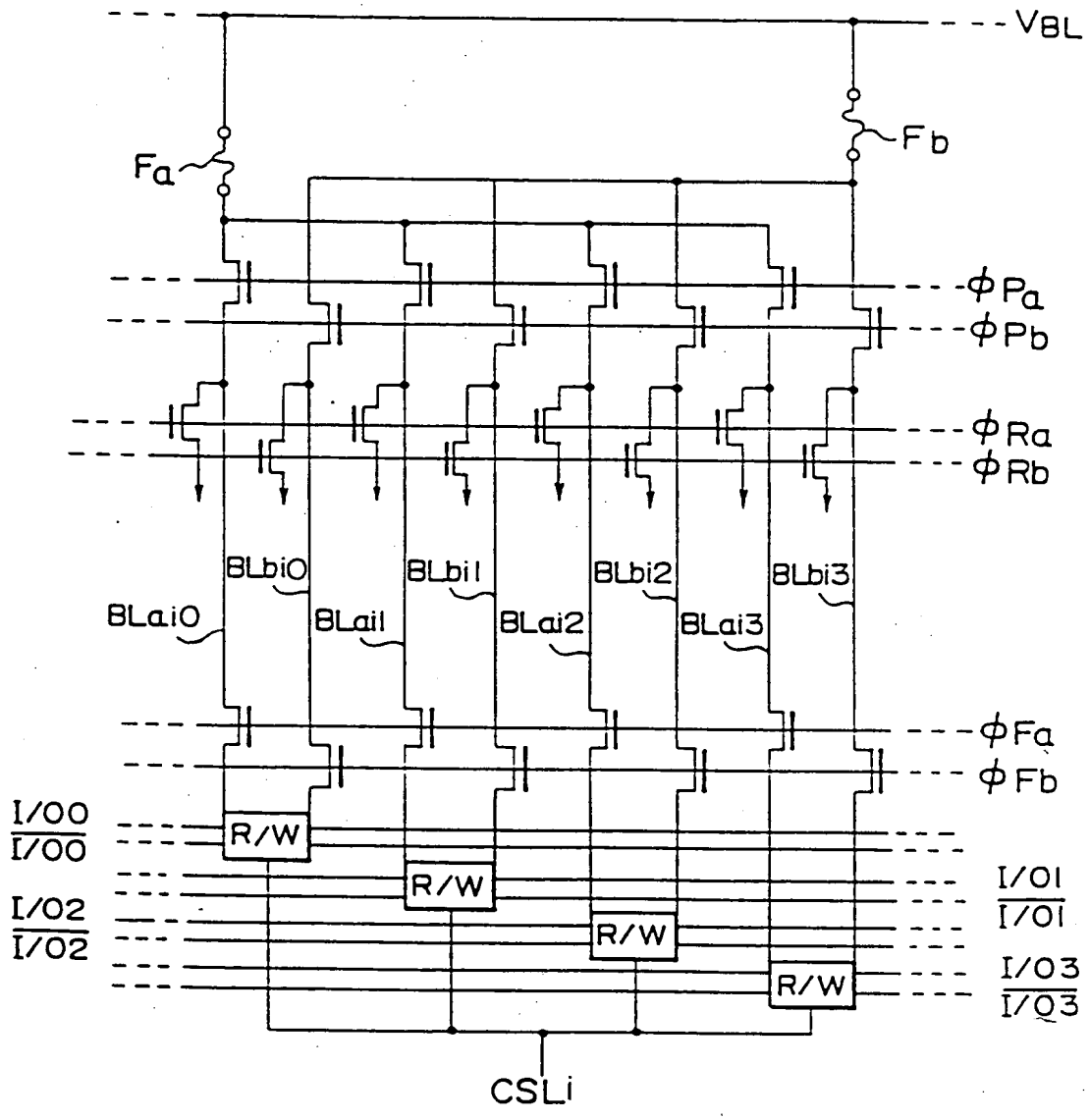

VBL
Fa
Fb
φPa
φPb
φRa
φRb
BLbi0
BLbi1
BLbi2
BLbi3
BLai0
BLai1
BLai2
BLai3
φFa
φFb
I/00
I/00
R/W
R/W
R/W
R/W
I/02
I/02
I/01
I/01
I/03
I/03
CSLi

FIG. 41

FIG. 42(a)

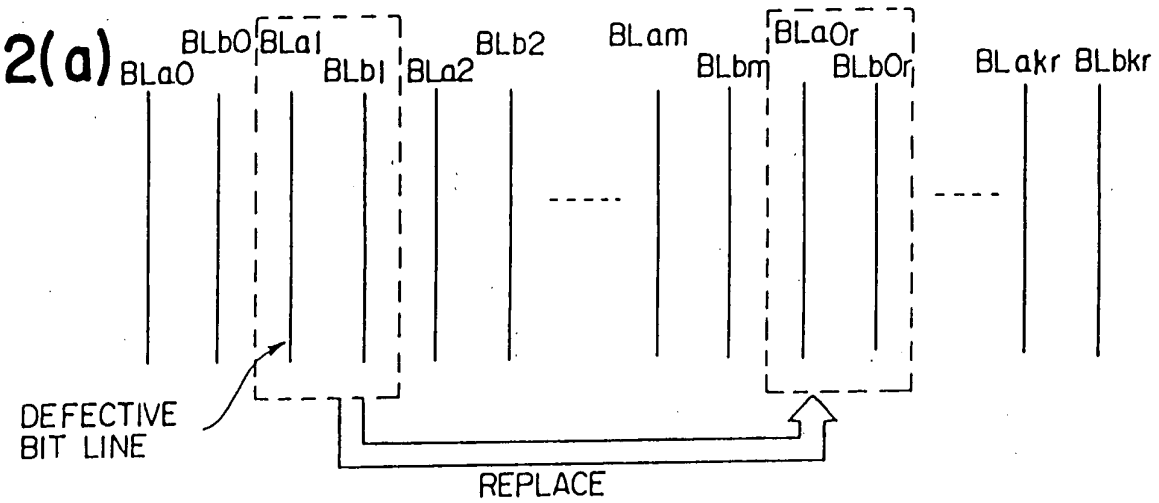
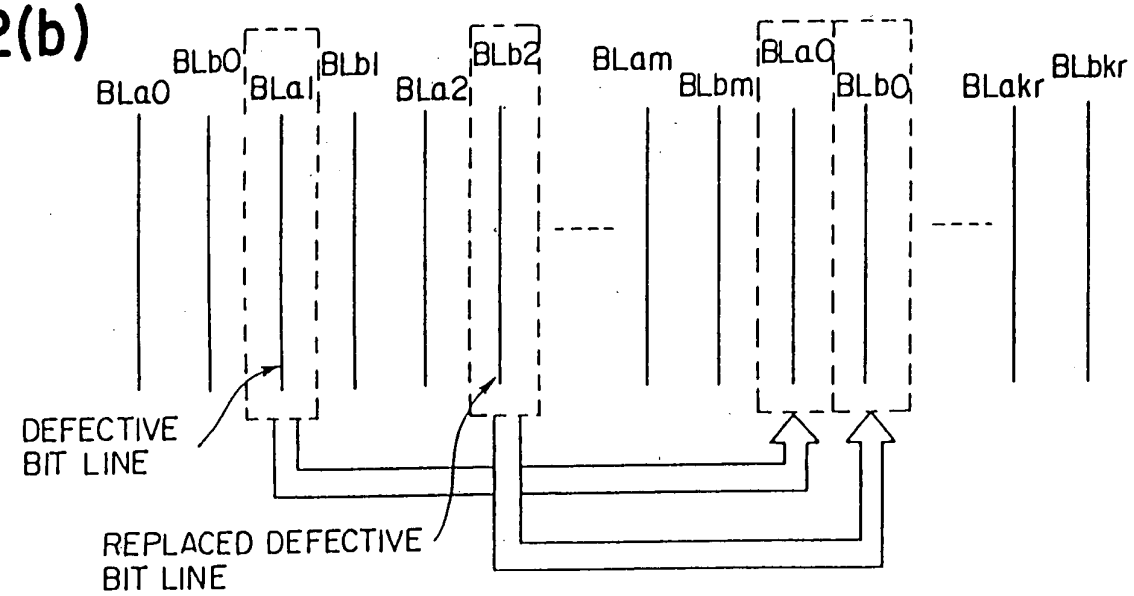


FIG. 42(b)



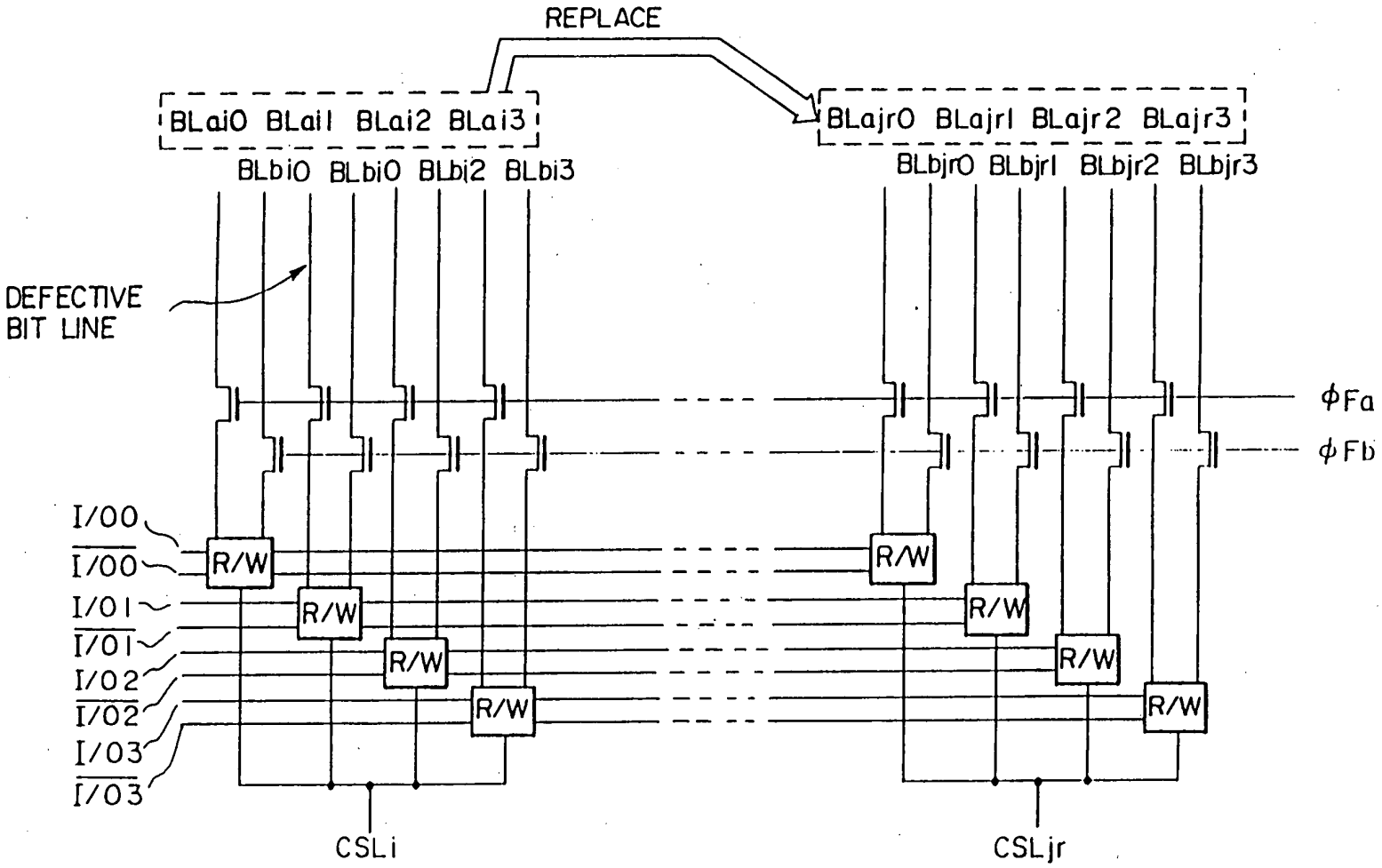

REPLACE
BLaiO BLail BLai2 BLai3
BLajrO BLajrl BLajr2 BLajr3
BLbiO BLbiO BLbi2 BLbi3
BLbjrO BLbjrl BLbjr2 BLbjr3
DEFECTIVE BIT LINE
φFa
φFb
I/00
I/00
I/01
I/01
I/02
I/02
I/03
I/03
R/W
CSLi
CSLjr

FIG. 43

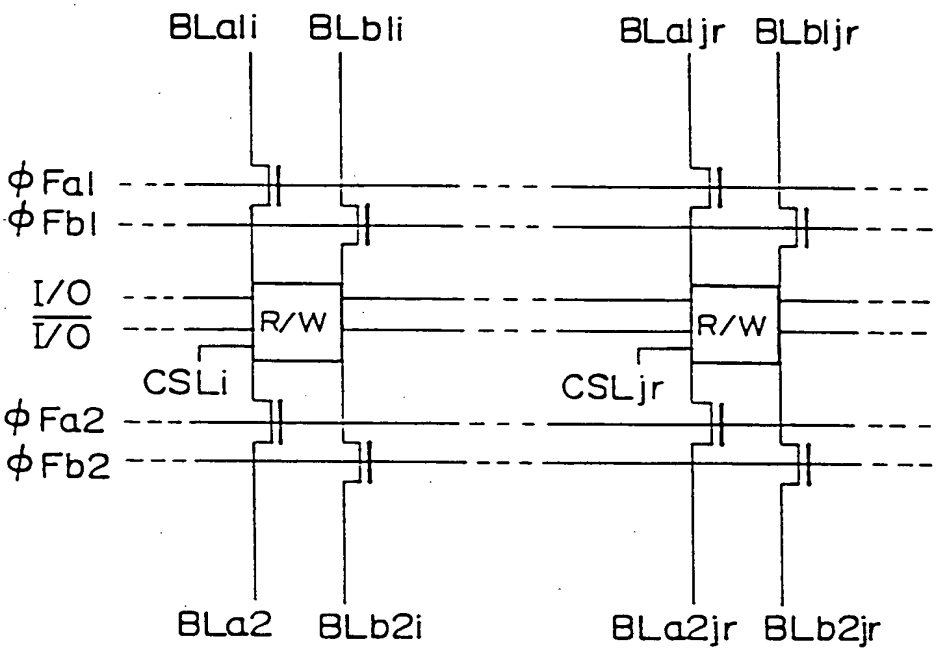

BLali
BLbli
BLaljr
BLbljr
φFal
φFbl
I/O
I/O
R/W
R/W
CSLi
CSLjr
φFa2
φFb2
BLa2
BLb2i
BLa2jr
BLb2jr

FIG. 44

FIG. 45(a)

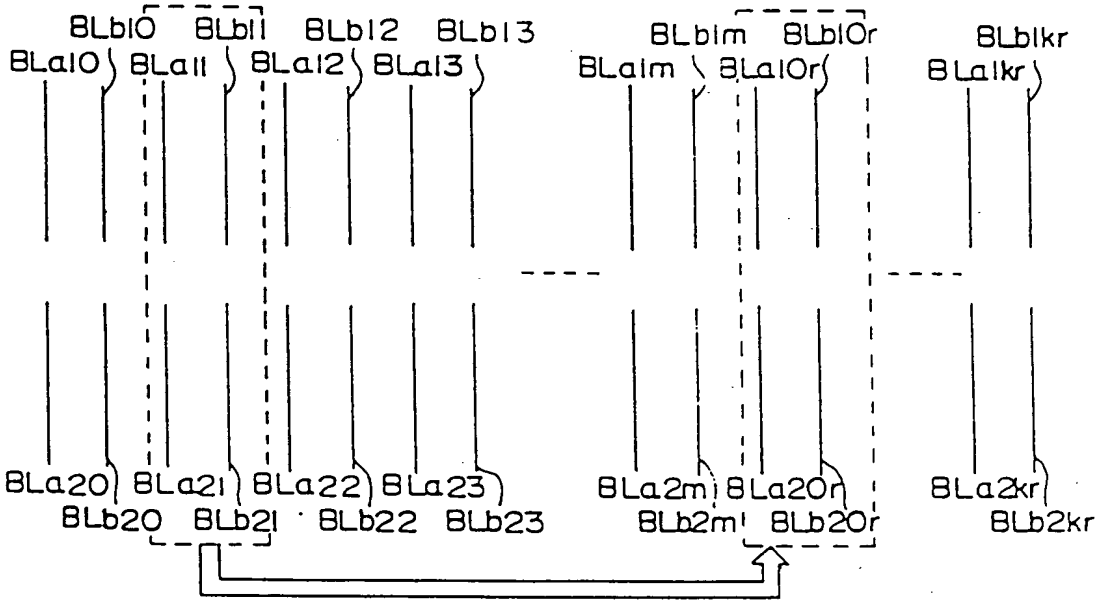


FIG. 45(b)

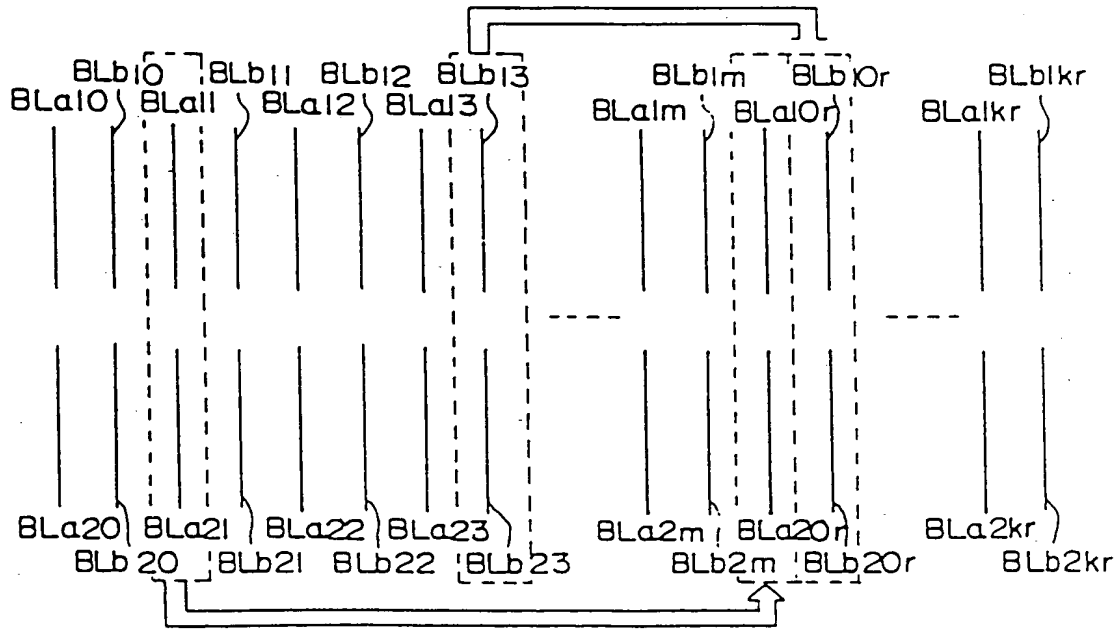


FIG. 46(a)

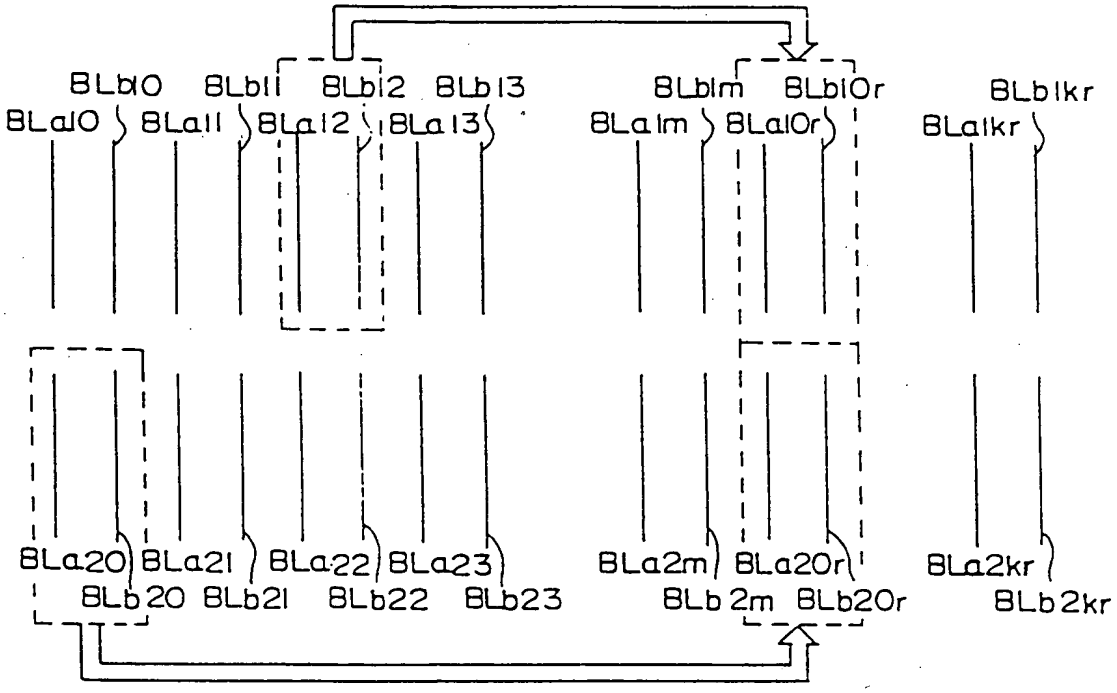
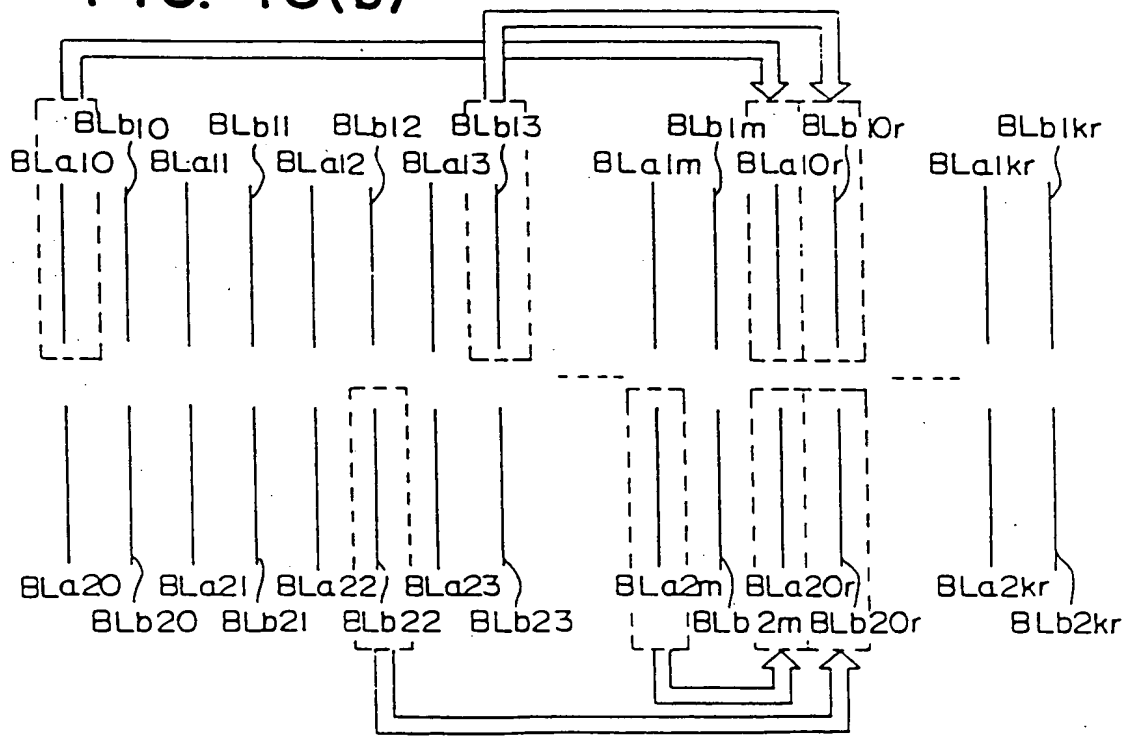


FIG. 46(b)



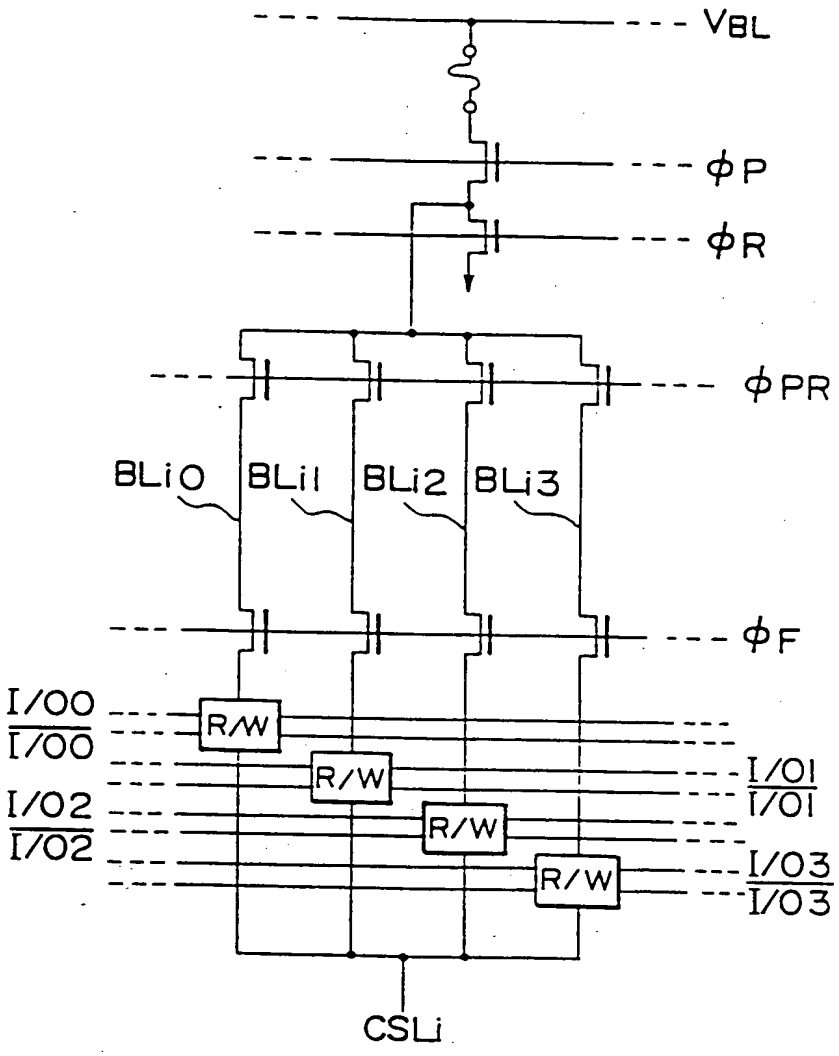

VBL
φP
φR
φPR
BLi0
BLi1
BLi2
BLi3
φF
I/00
I/00
I/02
I/02
R/W
R/W
R/W
R/W
I/01
I/01
I/03
I/03
CSLi

FIG. 47

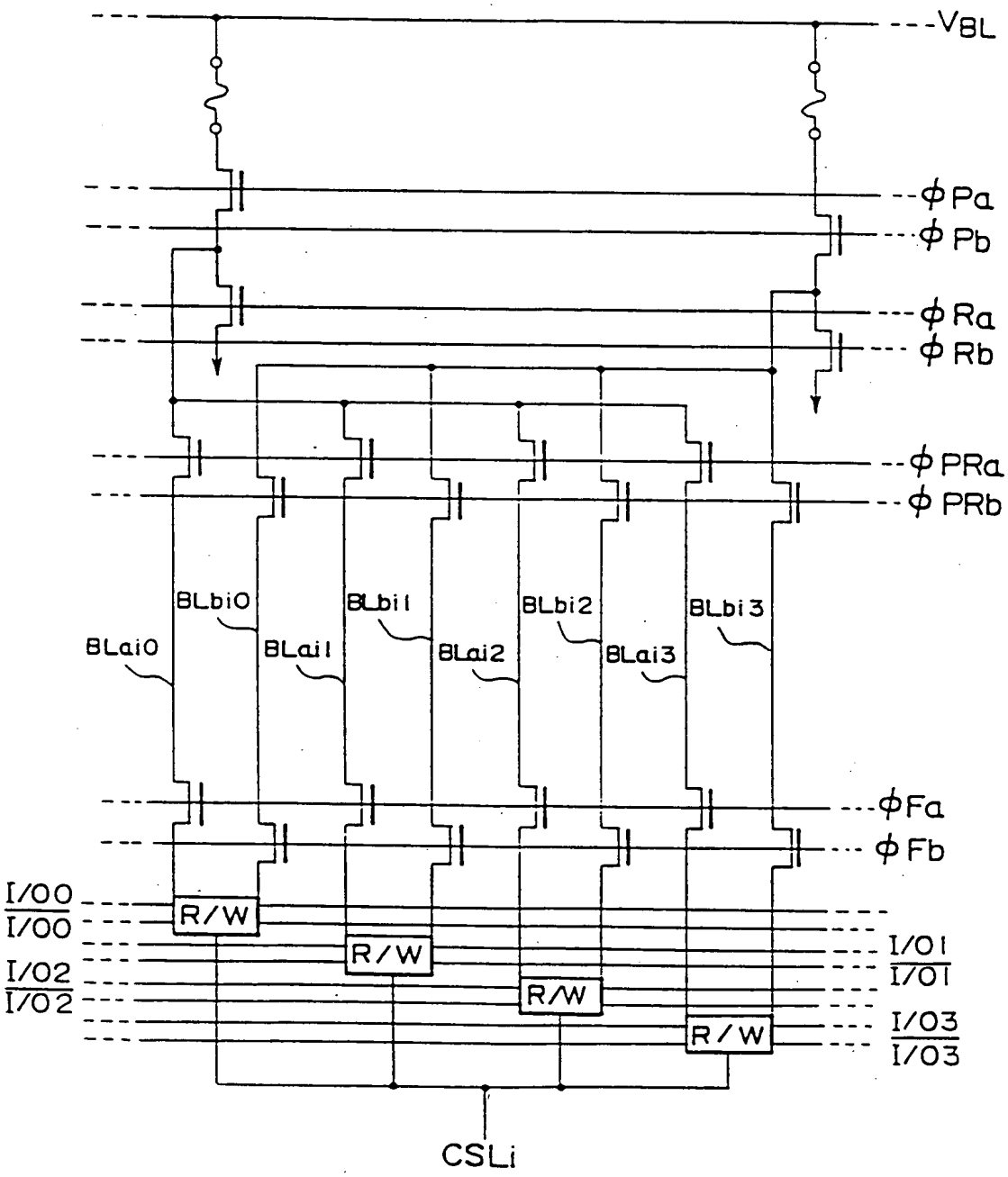

VBL
φPa
φPb
φRa
φRb
φPRa
φPRb
BLbi0
BLbi1
BLbi2
BLbi3
BLai0
BLai1
BLai2
BLai3
φFa
φFb
I/00
I/00
I/02
I/02
R/W
R/W
R/W
R/W
I/01
I/01
I/03
I/03
CSLi

FIG. 48

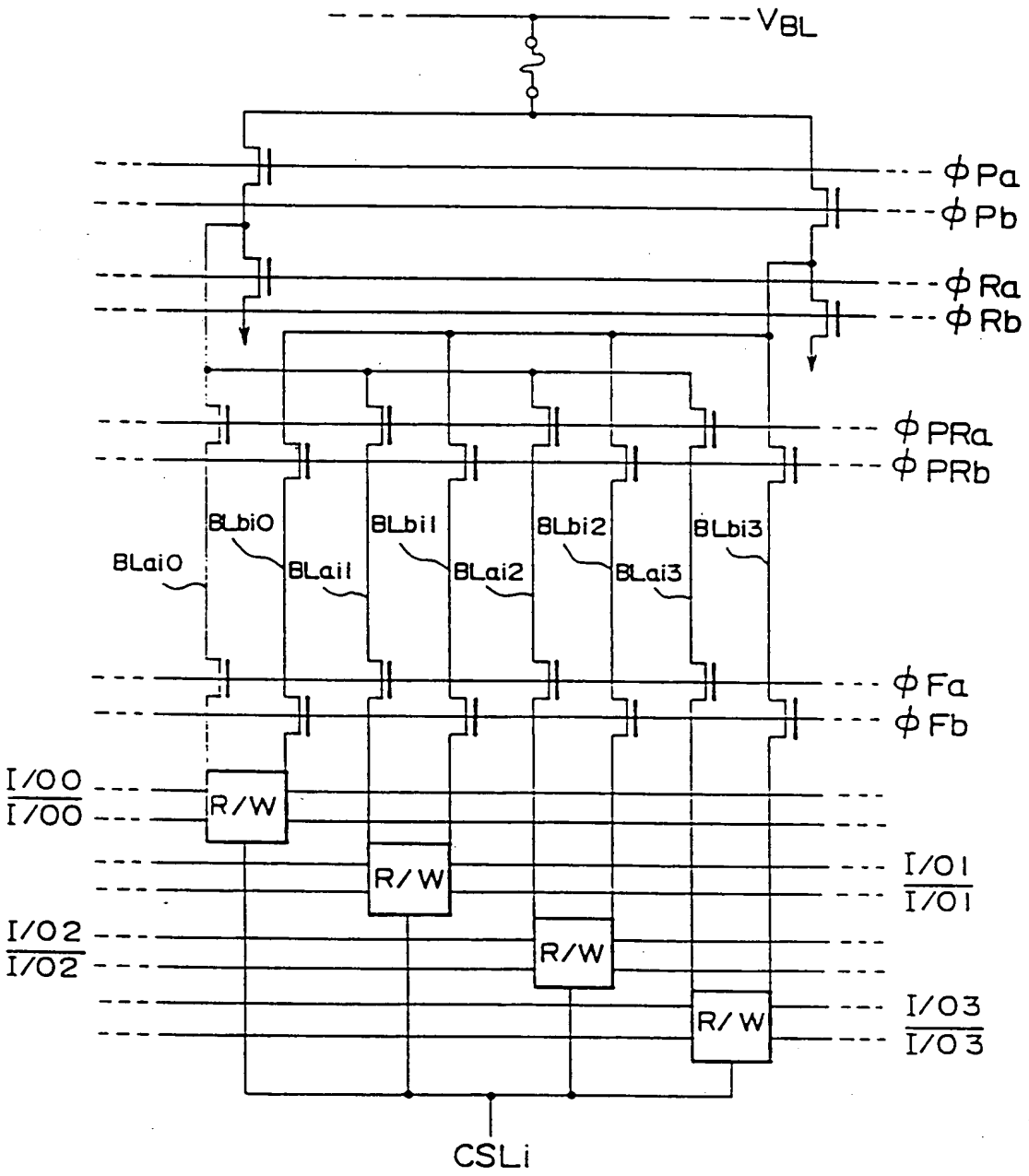

VBL
φPa
φPb
φRa
φRb
φPRa
φPRb
BLbi0
BLbi1
BLbi2
BLbi3
BLai0
BLai1
BLai2
BLai3
φFa
φFb
I/00
I/00
R/W
R/W
R/W
R/W
I/01
I/01
I/02
I/02
I/03
I/03
CSLi

FIG. 49

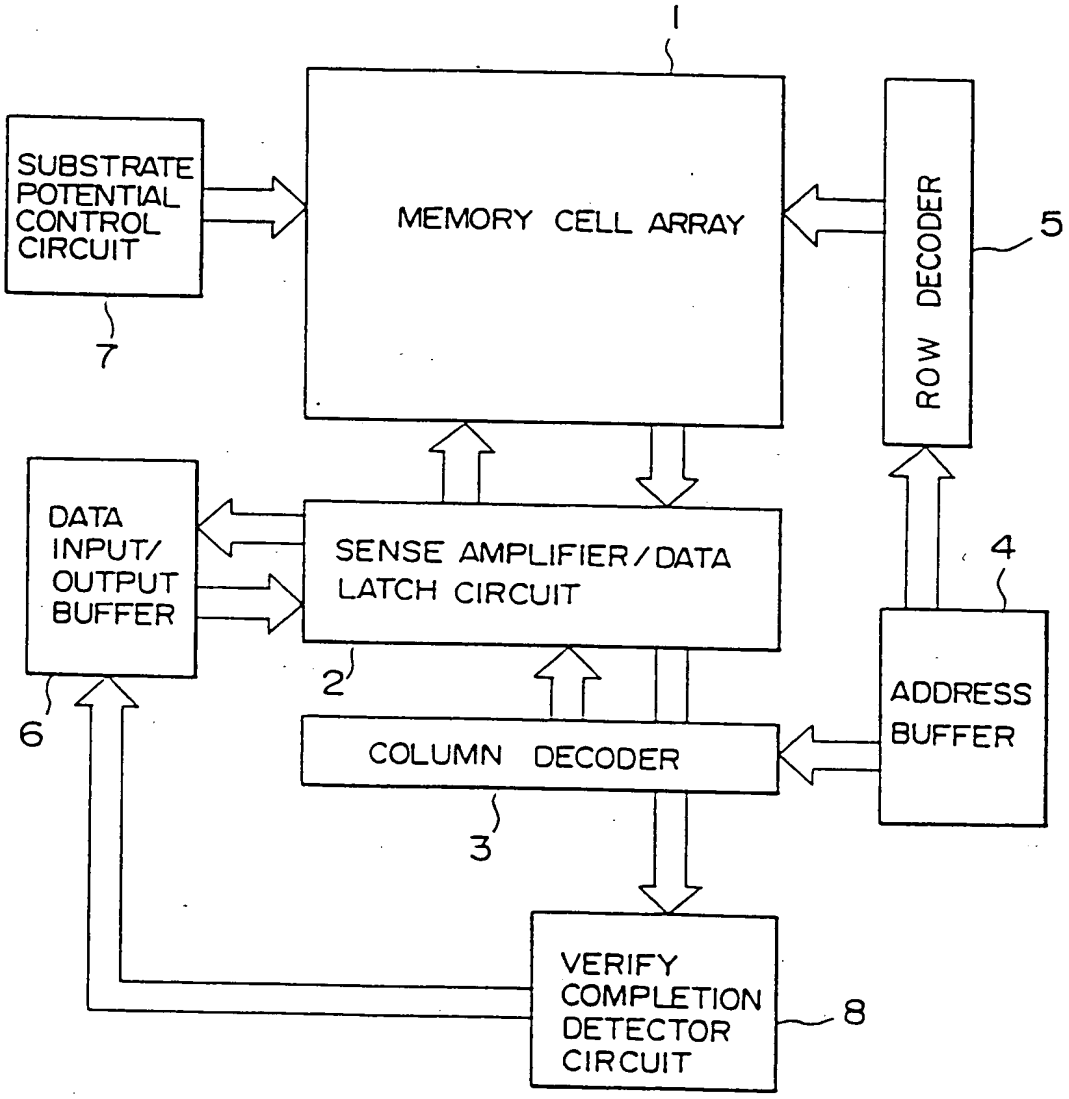

1
SUBSTRATE POTENTIAL CONTROL CIRCUIT
MEMORY CELL ARRAY
ROW DECODER
5
7
DATA INPUT/ OUTPUT BUFFER
SENSE AMPLIFIER/DATA LATCH CIRCUIT
4
2
6
ADDRESS BUFFER
COLUMN DECODER
3
VERIFY COMPLETION DETECTOR CIRCUIT
8

FIG.50

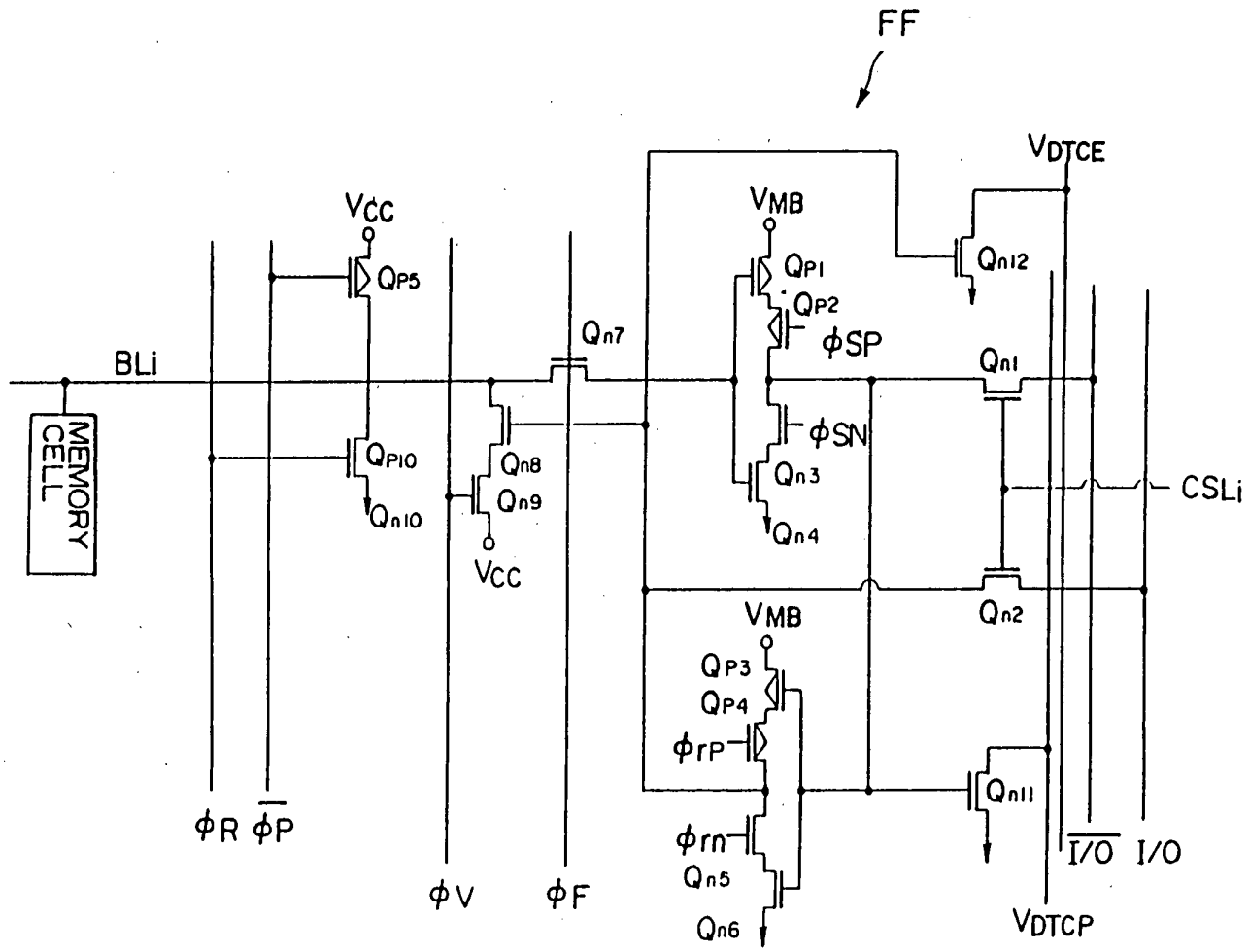

FF
VDTCE
VCC
VMB
QP1
QP2
φSP
Qn12
Qn7
BLi
Qn1
MEMORY CELL
QP5
φSN
CSLi
QP10
Qn8
Qn3
Qn10
Qn9
Qn4
VCC
VMB
Qn2
QP3
QP4
φrP
Qn11
φR φP
φrn
I/O I/O
φV
φF
Qn5
Qn6
VDTCP

FIG. 51

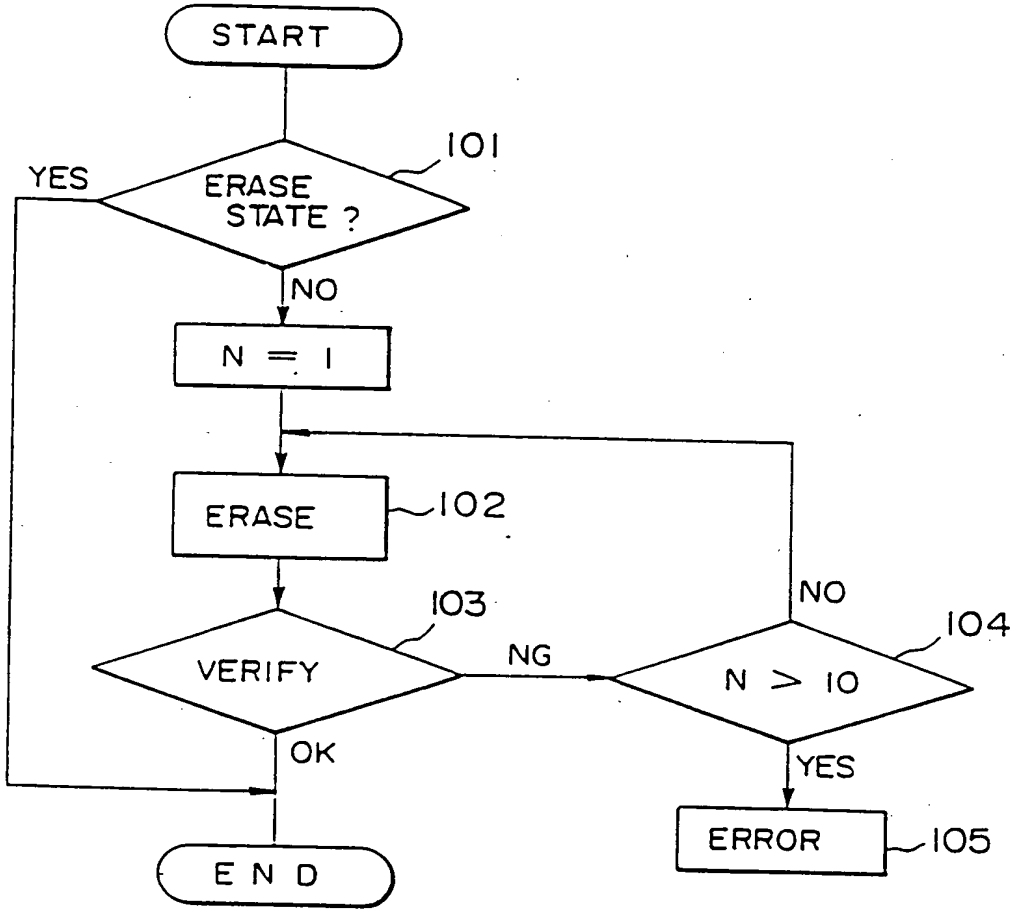

START
101
YES
ERASE STATE ?
NO
N = 1
ERASE
102
103
NO
104
VERIFY
NG
N > 10
OK
YES
ERROR
105
E N D

FIG. 52

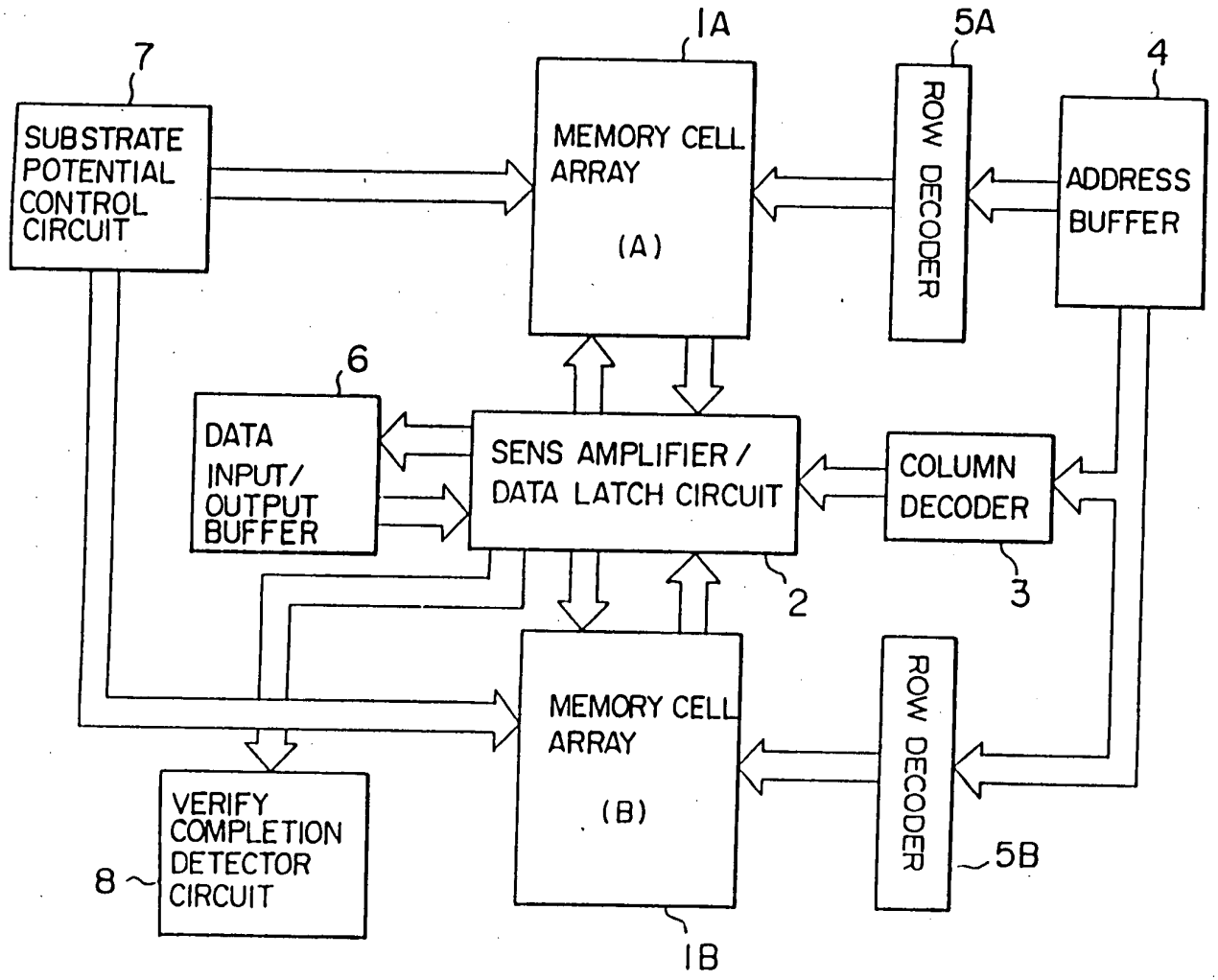

7
SUBSTRATE POTENTIAL CONTROL CIRCUIT
1A
MEMORY CELL ARRAY (A)
5A
ROW DECODER
4
ADDRESS BUFFER
6
DATA INPUT/ OUTPUT BUFFER
SENS AMPLIFIER / DATA LATCH CIRCUIT
COLUMN DECODER
2
3
MEMORY CELL ARRAY (B)
ROW DECODER
5B
VERIFY COMPLETION DETECTOR CIRCUIT
8
1B

FIG. 53

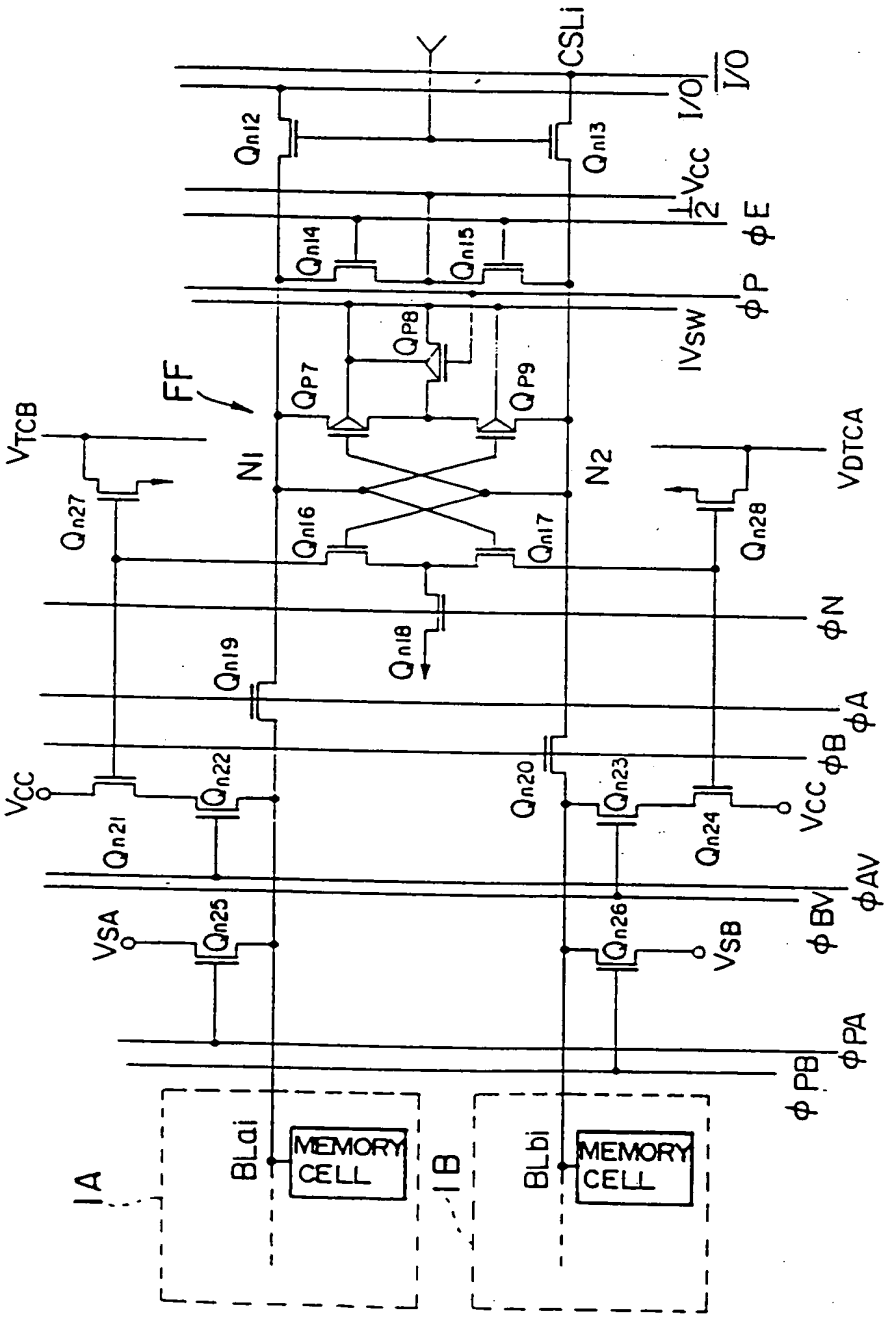

CSLi
I/O
$\overline{I/O}$
Q_{n12}
Q_{n13}
$\frac{1}{2}V_{CC}$
ϕE
Q_{n14}
Q_{n15}
ϕP
V_{SW}
Q_{P8}
Q_{P7}
Q_{P9}
FF
V_{TCB}
N1
N2
V_{DTCA}
Q_{n27}
Q_{n16}
Q_{n17}
Q_{n28}
ϕN
Q_{n18}
Q_{n19}
ϕA
ϕB
V_{CC}
Q_{n20}
Q_{n22}
Q_{n23}
V_{CC}
Q_{n21}
Q_{n24}
ϕAV
V_{SA}
Q_{n25}
Q_{n26}
V_{SB}
ϕBV
ϕPA
ϕPB
IA
BLai
MEMORY CELL
IB
BLbi
MEMORY CELL

FIG. 54

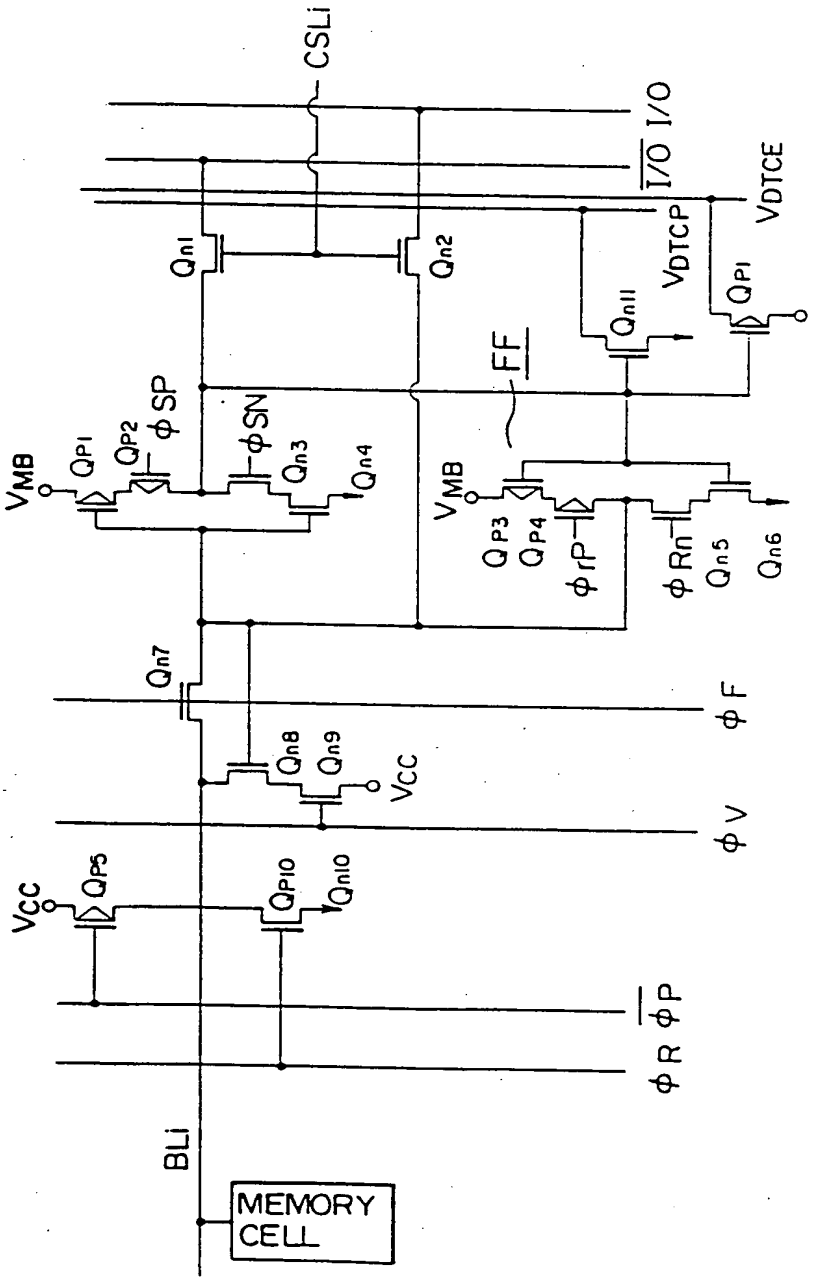

CSLi
I/O
$\overline{I/O}$
VDTCE
VDTCP
QP1
Qn11
Qn1
Qn2
FF
VMB
QP1
QP2
φSP
φSN
Qn3
Qn4
VMB
QP3
QP4
φrP
φRn
Qn5
Qn6
Qn7
φF
Qn8
Qn9
VCC
φV
VCC
QP5
QP10
Qn10
$\overline{\phi R}$
$\overline{\phi P}$
BLi
MEMORY CELL

FIG.55

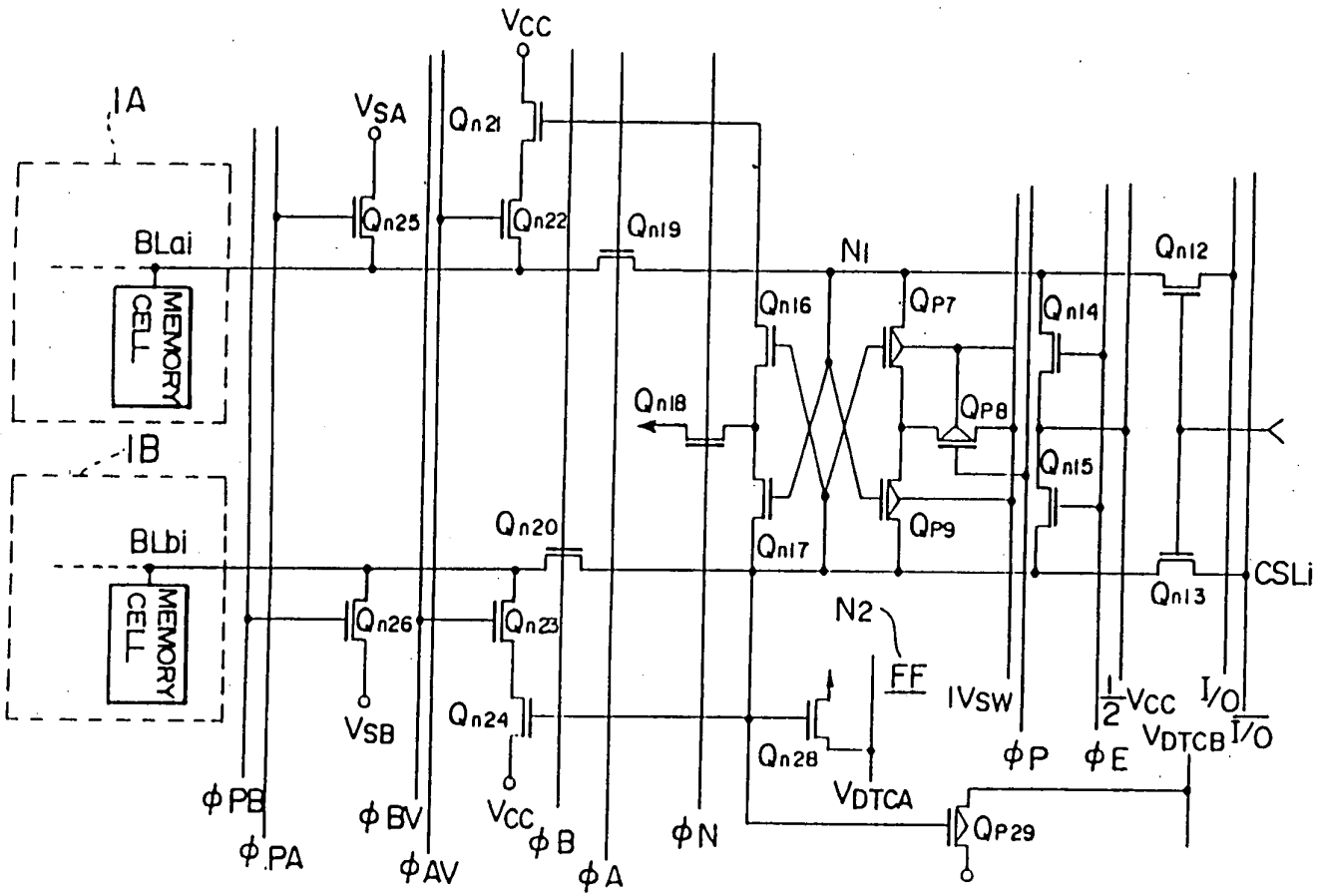

VCC
IA
VSA
Qn21
Qn25
Qn22
Qn19
BLai
MEMORY CELL
N1
Qn12
Qn16
QP7
Qn14
Qn18
QP8
IB
Qn15
BLbi
Qn20
Qn17
QP9
CSLi
Qn13
N2
Qn26
Qn23
FF
IVSW
1/2 VCC
I/O
Qn24
VSB
Qn28
VDTCB
I/O
φP
φE
VDTCA
φPB
φBV
VCC
QP29
φB
φN
φPA
φAV
φA

FIG. 56

FIG. 57(a)

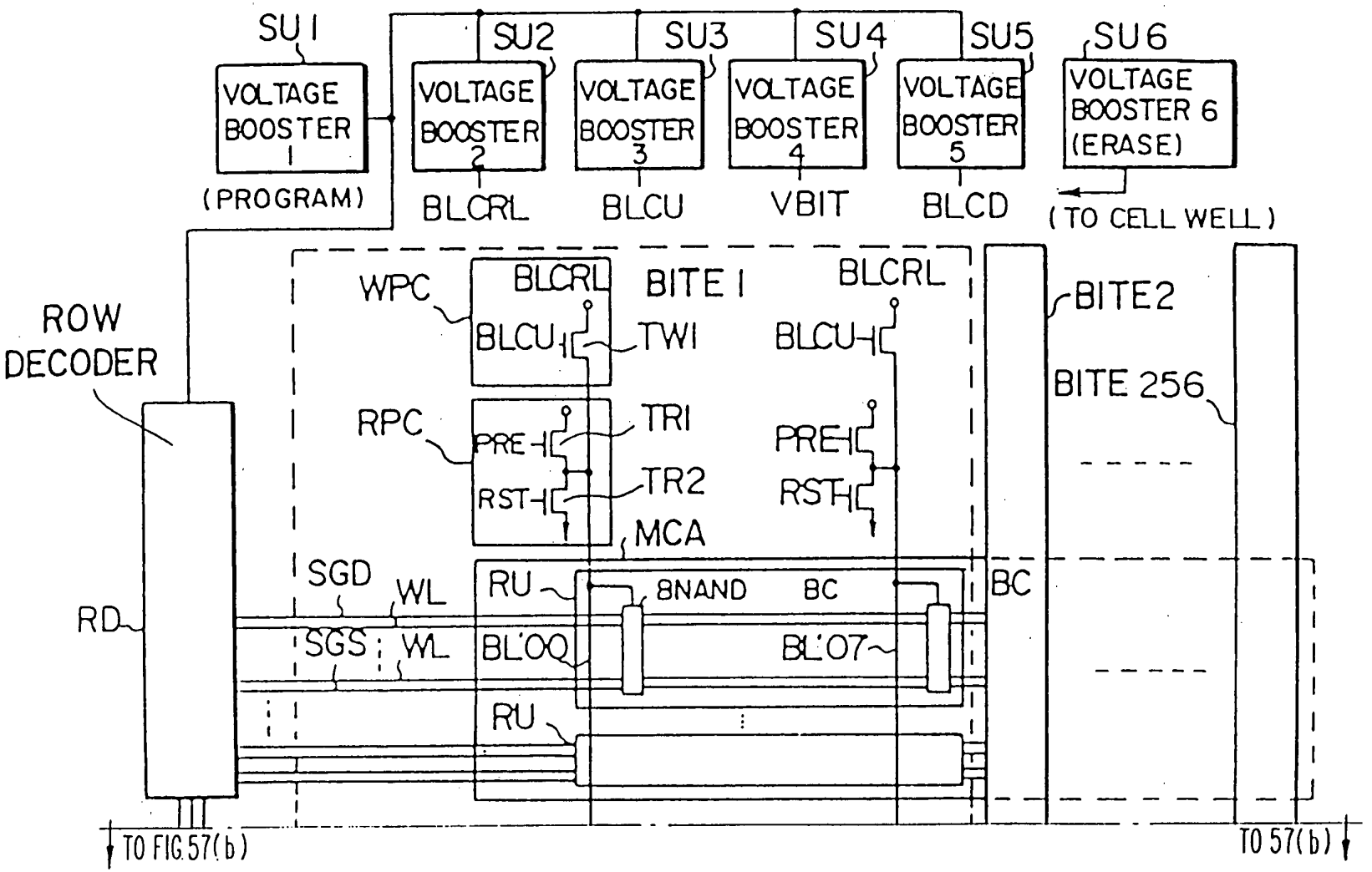

SU1
SU2
SU3
SU4
SU5
SU6
VOLTAGE BOOSTER 1
VOLTAGE BOOSTER 2
VOLTAGE BOOSTER 3
VOLTAGE BOOSTER 4
VOLTAGE BOOSTER 5
VOLTAGE BOOSTER 6 (ERASE)
(PROGRAM)
BLCRL
BLCU
VBIT
BLCD
(TO CELL WELL)
ROW DECODER
WPC
BLCRL
BITE 1
BLCRL
BITE2
BLCU
TWI
BLCU
BITE 256
RPC
TRI
PRE
PRE
TR2
RST
RST
MCA
SGD
WL
RU
8NAND
BC
BC
RD
SGS
WL
BL'0Q
BL'07
RU
TO FIG.57(b)
TO 57(b)

FIG. 57(b)

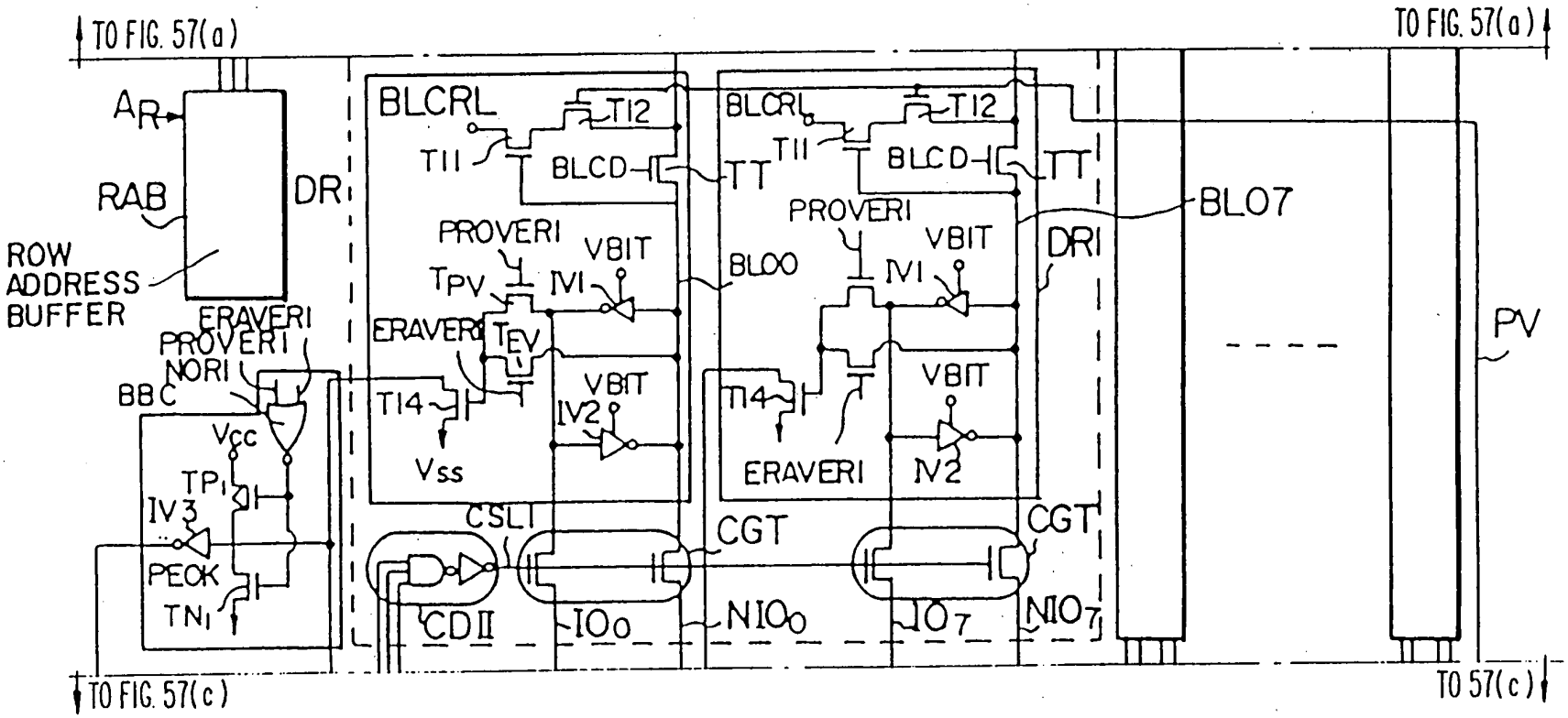
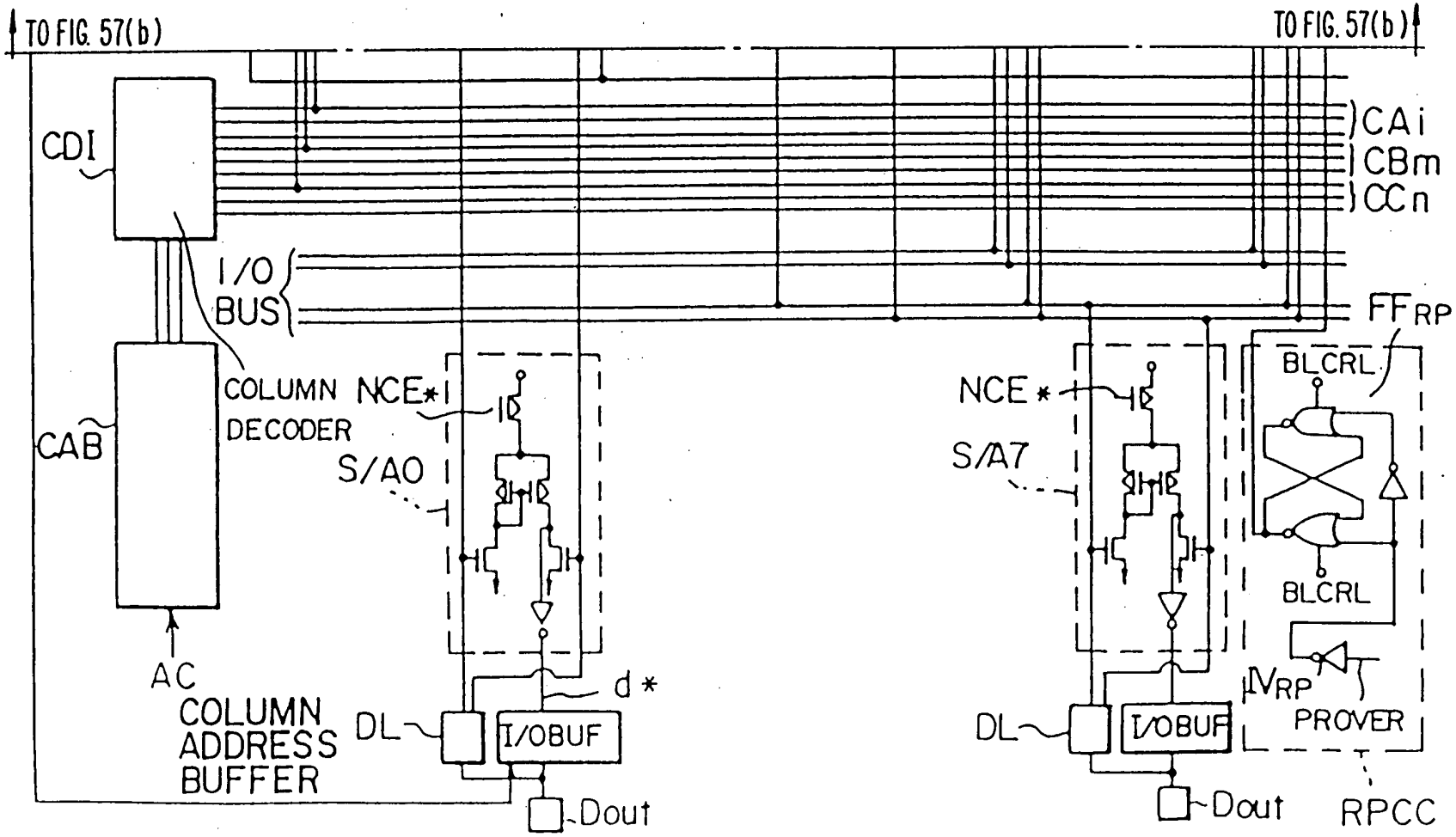

TO FIG. 57(a)
TO FIG. 57(a)
AR
RAB
DR
ROW ADDRESS BUFFER
ERAVERI
PROVERI
NORI
BBC
Vcc
TP1
IV3
PEOK
TN1
BLCRL
T12
T11
BLCD
TT
PROVERI
VBIT
TPV
IV1
BLOO
ERAVERI
TEV
T14
Vss
IV2
CSLI
CDII
IOo
CGT
NIOo
BLCRL
T12
T11
BLCD
TT
PROVERI
VBIT
IV1
DRI
BLO7
T14
ERAVERI
IV2
CGT
IO7
NIO7
PV
TO FIG. 57(c)
TO 57(c)

FIG. 57(c)


TO FIG. 57(b)
TO FIG. 57(b)
CDI
CAB
AC
COLUMN ADDRESS BUFFER
I/O BUS
COLUMN DECODER
NCE*
S/A0
d*
DL
I/OBUF
Dout
CAi
CBm
CCn
FFRP
NCE*
S/A7
BLCRL
BLCRL
μVRP
PROVER
RPCC
DL
I/OBUF
Dout

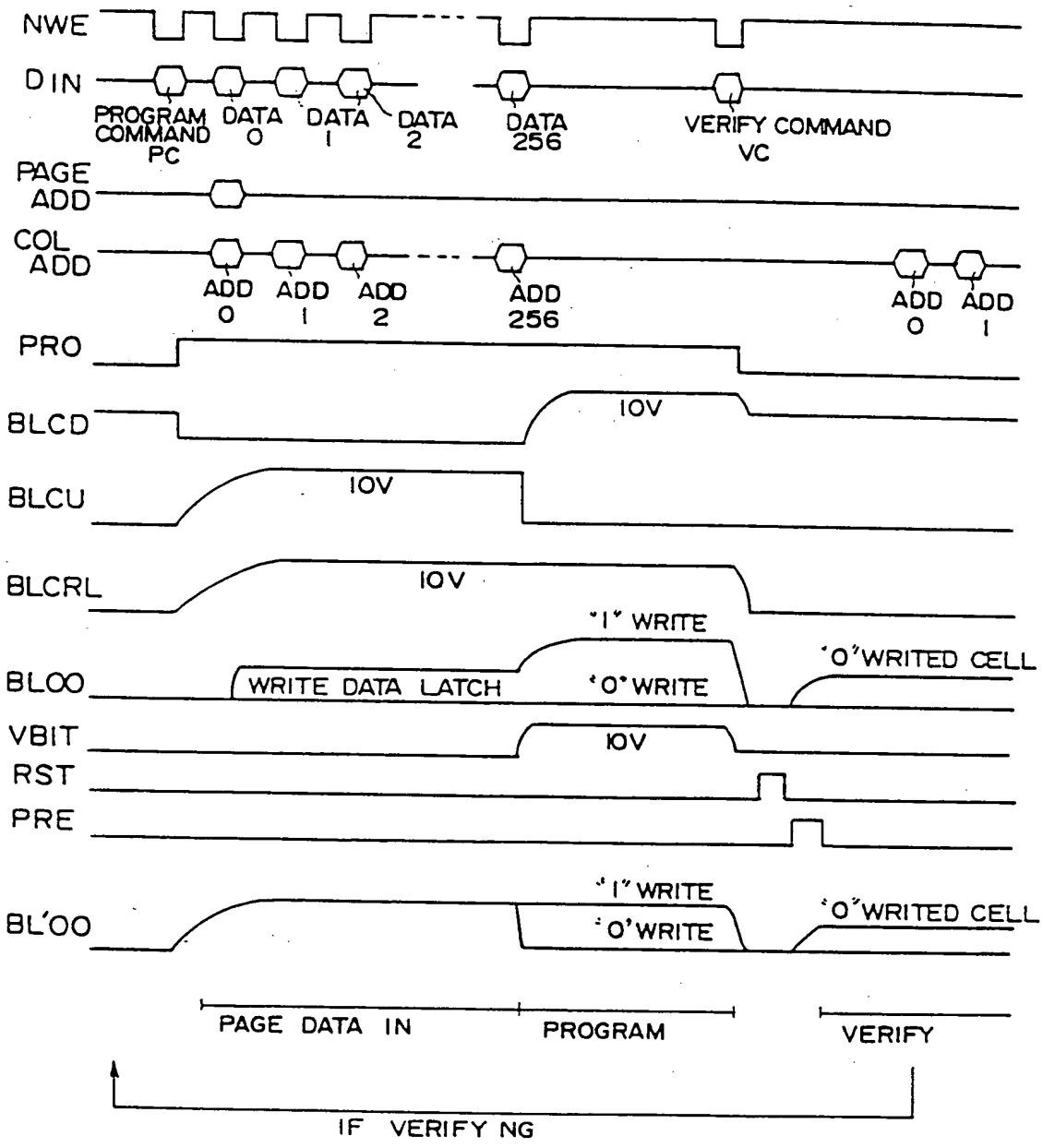

NWE
DIN
PROGRAM COMMAND PC
DATA 0
DATA 1
DATA 2
DATA 256
VERIFY COMMAND VC
PAGE ADD
COL ADD
ADD 0
ADD 1
ADD 2
ADD 256
ADD 0
ADD 1
PRO
BLCD
10V
BLCU
10V
BLCRL
10V
"1" WRITE
"0"WRITED CELL
BLOO
WRITE DATA LATCH
"0" WRITE
VBIT
10V
RST
PRE
"1" WRITE
BL'OO
"0" WRITE
"0"WRITED CELL
PAGE DATA IN
PROGRAM
VERIFY
IF VERIFY NG

FIG. 58

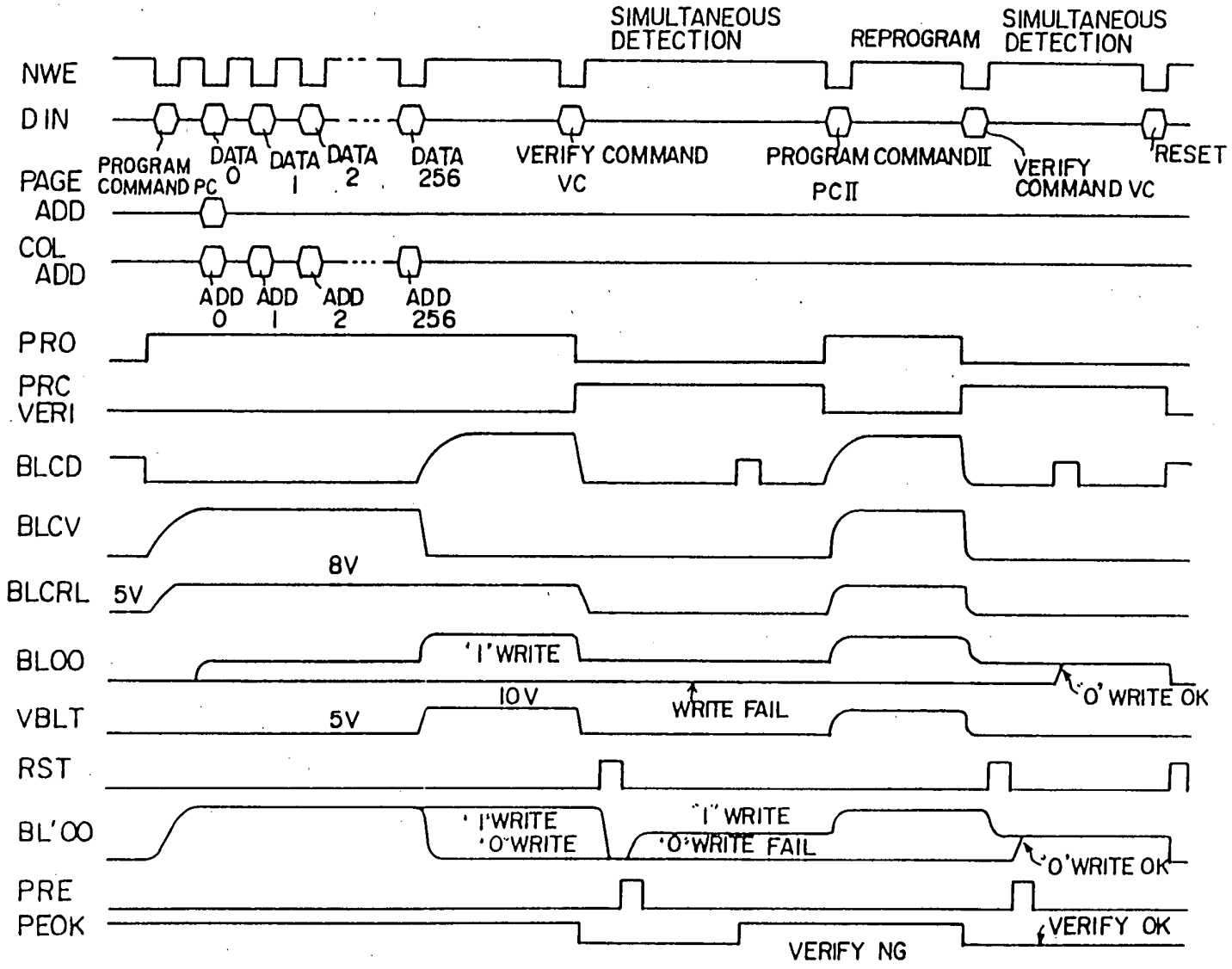

SIMULTANEOUS DETECTION
REPROGRAM
SIMULTANEOUS DETECTION
NWE
D IN
PROGRAM COMMAND PC
DATA 0
DATA 1
DATA 2
DATA 256
VERIFY COMMAND VC
PROGRAM COMMANDII PCII
VERIFY COMMAND VC
RESET
PAGE ADD
COL ADD
ADD 0
ADD 1
ADD 2
ADD 256
PRO
PRC VERI
BLCD
BLCV
8V
BLCRL
5V
BLOO
'1'WRITE
'0' WRITE OK
10V
VBLT
5V
WRITE FAIL
RST
BL'OO
'1'WRITE
'0'WRITE
'1'' WRITE
'0'WRITE FAIL
'0'WRITE OK
PRE
PEOK
VERIFY OK
VERIFY NG

FIG. 59

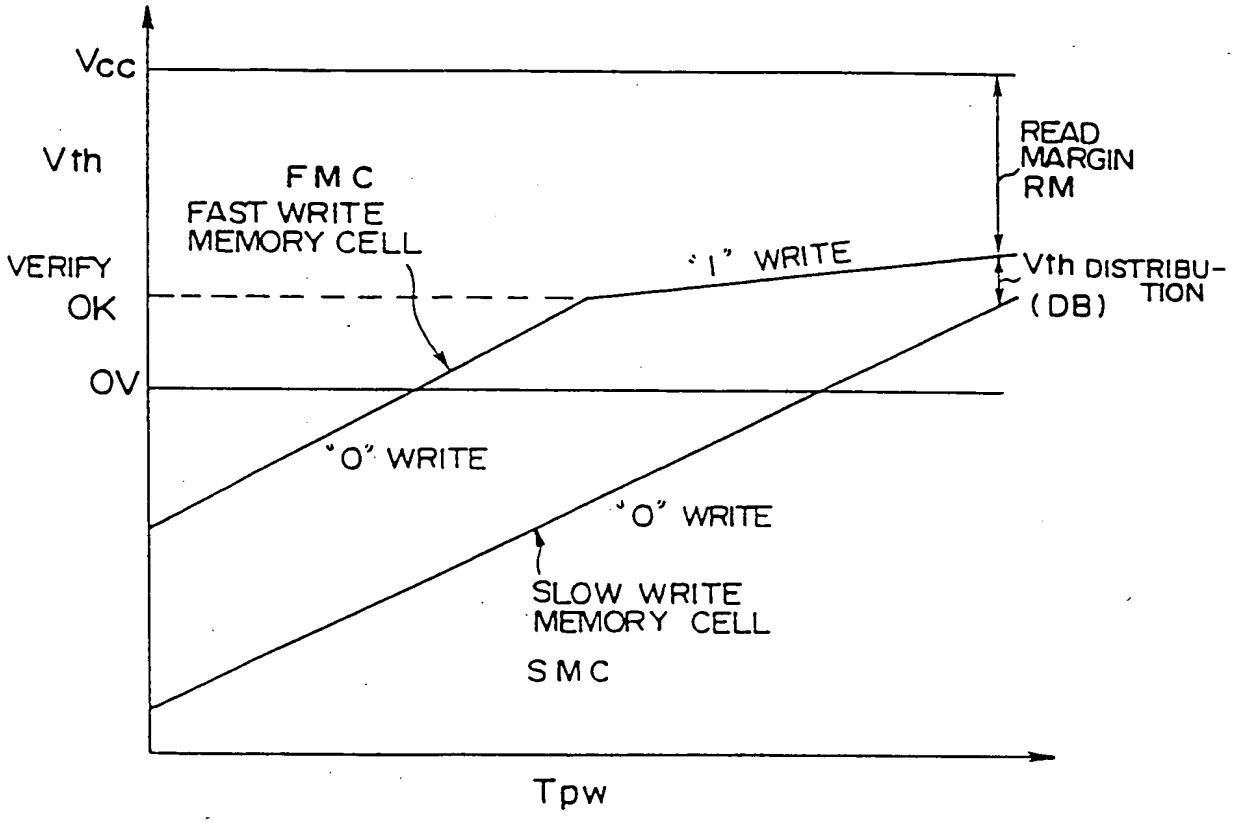

Vcc
Vth
FMC
FAST WRITE
MEMORY CELL
READ
MARGIN
RM
VERIFY
OK
"1" WRITE
Vth DISTRIBU-
TION
(DB)
OV
"0" WRITE
"0" WRITE
SLOW WRITE
MEMORY CELL
SMC
Tpw

FIG. 60

(ERASE FLOW CHART)

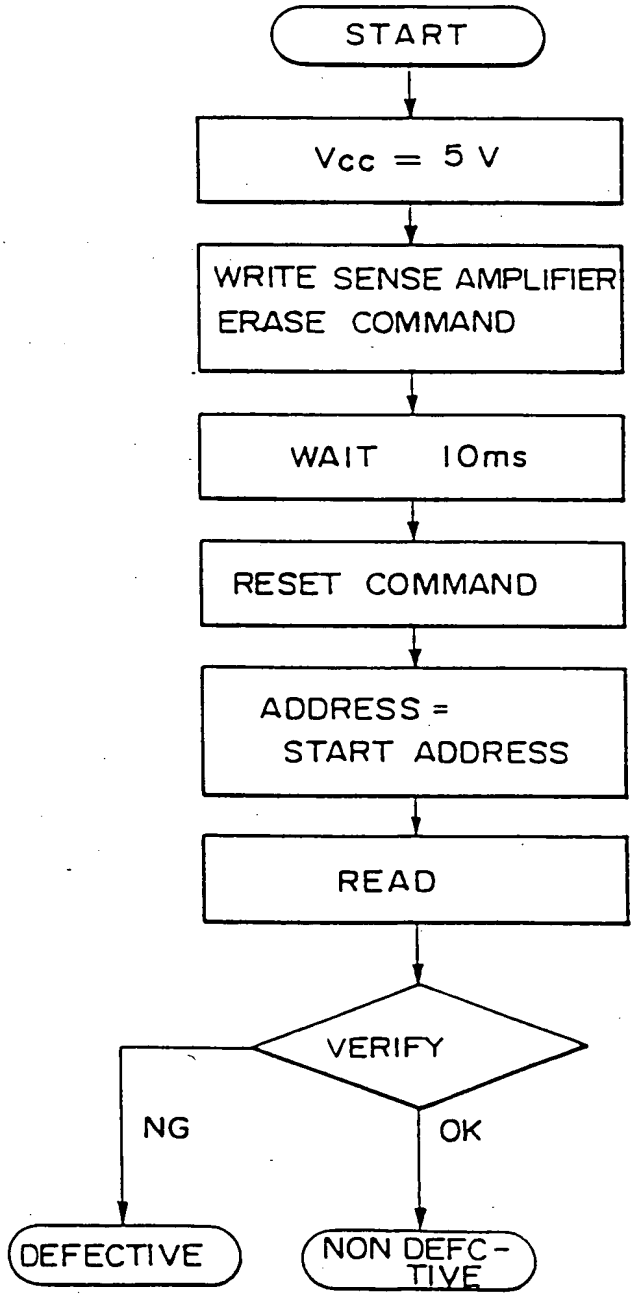


FIG. 61

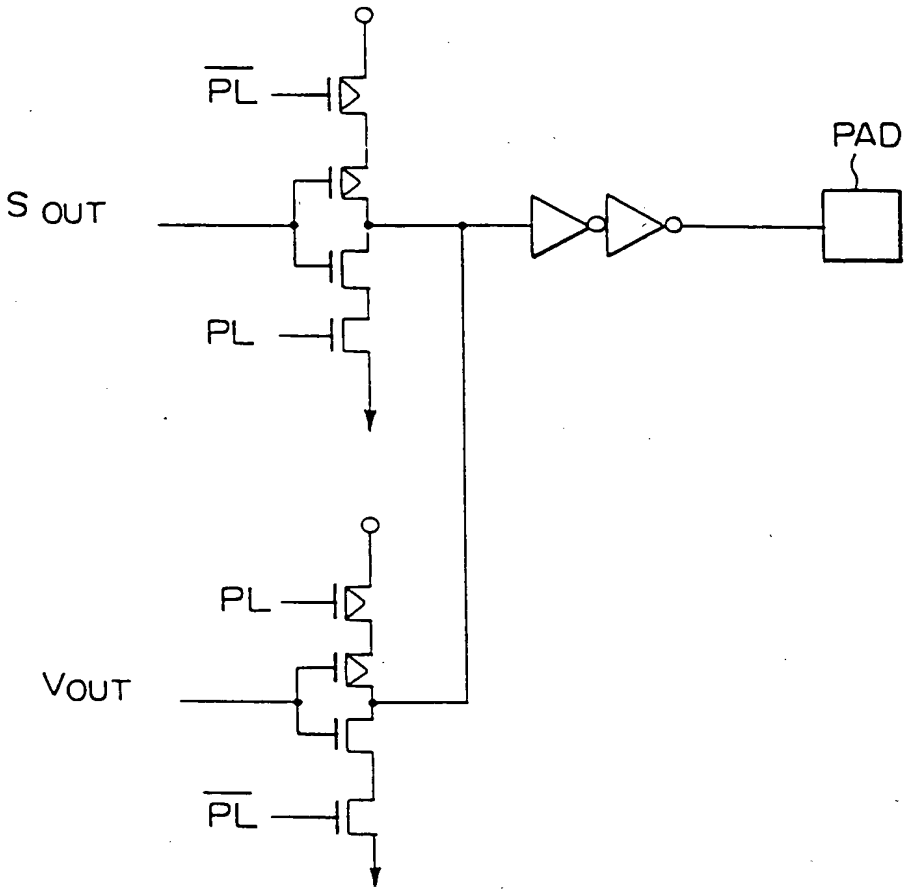


FIG. 62

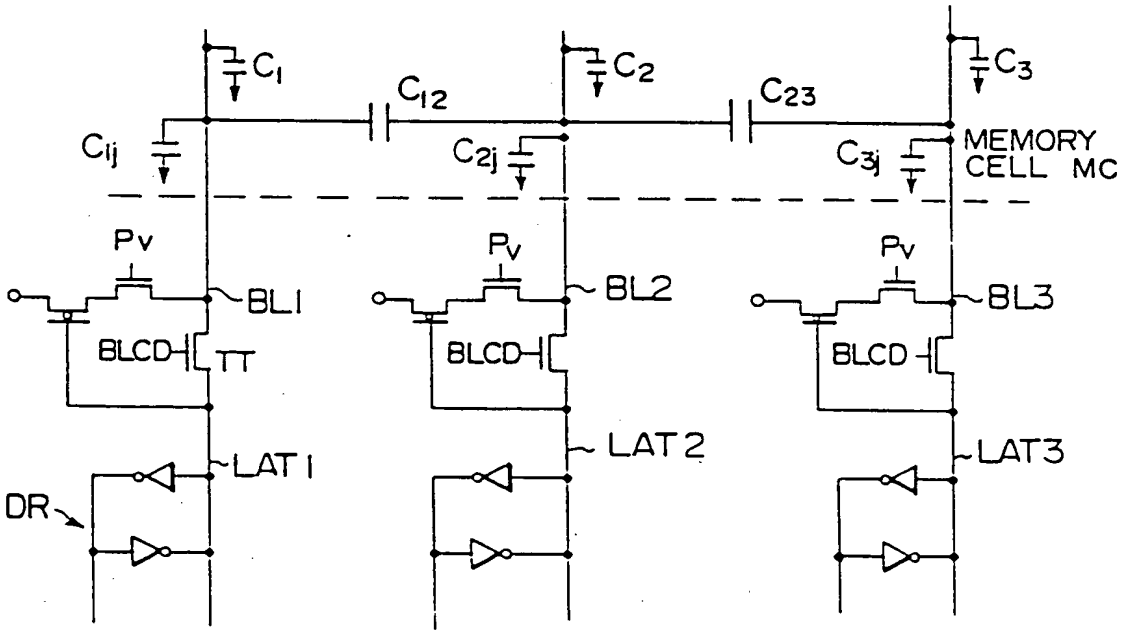

C1
C12
C2
C23
C3
C1j
C2j
C3j
MEMORY
CELL MC
Pv
Pv
Pv
BL1
BL2
BL3
BLCD
TT
BLCD
BLCD
LAT1
LAT2
LAT3
DR

FIG. 63

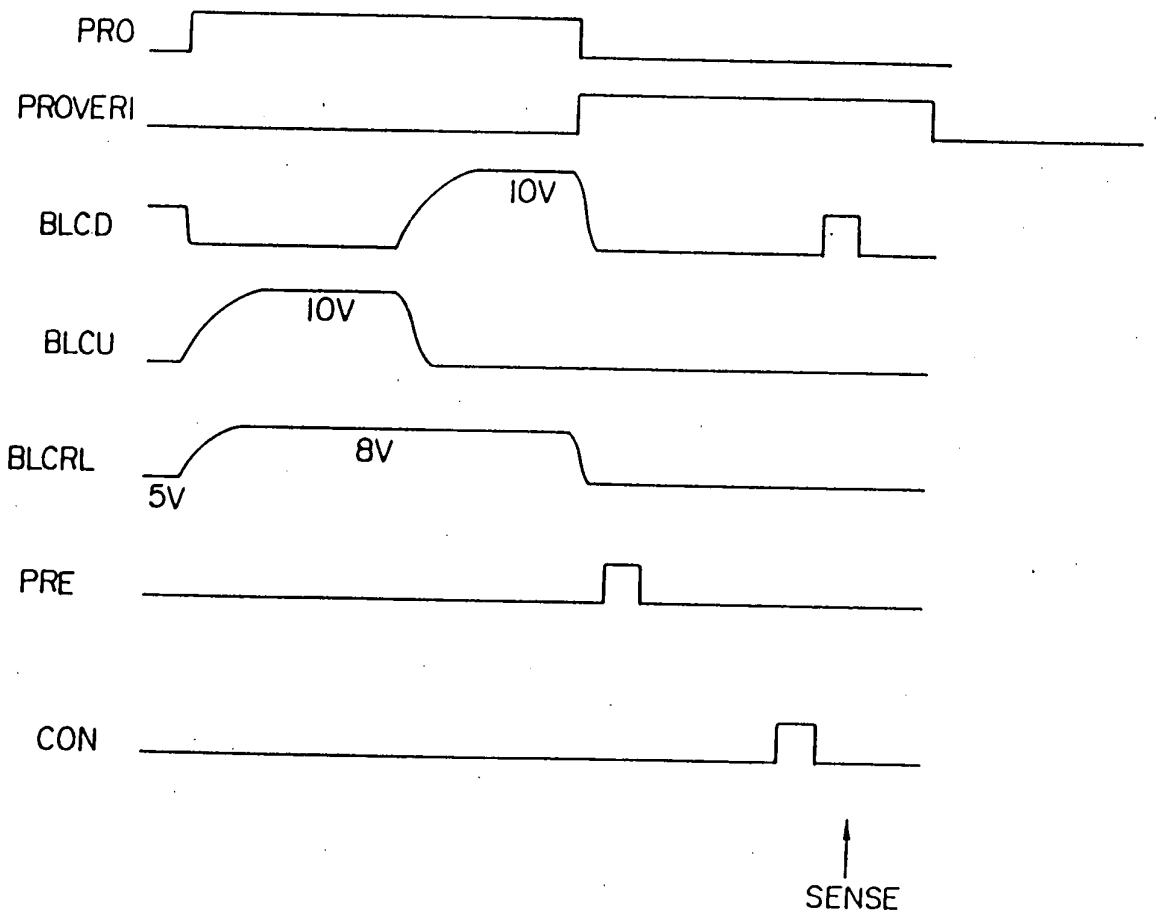


FIG.64

FIG. 65(a)

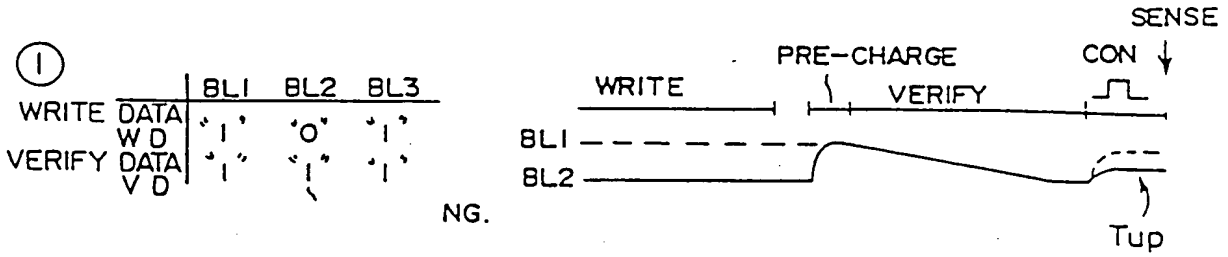


FIG. 65(b)

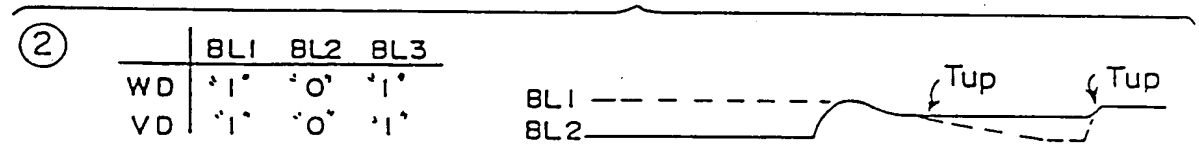


FIG. 65(c)

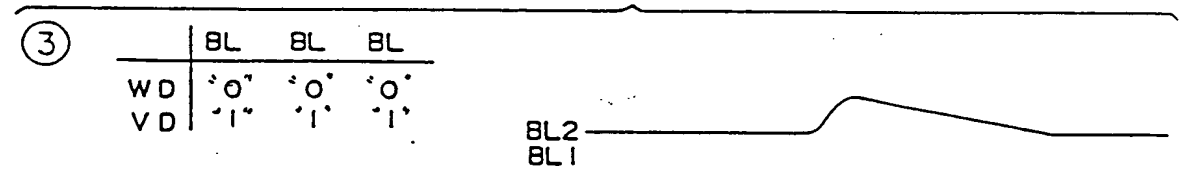


FIG. 65(d)

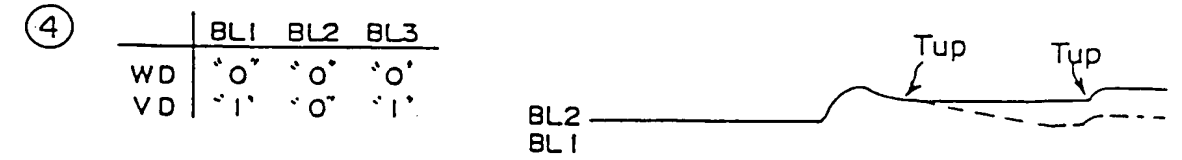


FIG. 65(e)

⑤

	BL1	BL2	BL3
WD	"0"	"0"	"0"
VD	"0"	"1"	"0"

FIG. 65(f)

⑥

	BL1	BL2	BL3
WD	"0"	"0"	"0"
VD	"0"	"0"	"0"

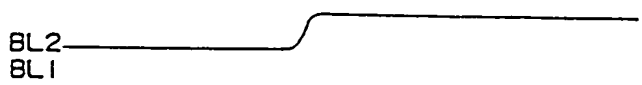


FIG. 65(g)

⑦

	BL1	BL2	BL3
WD	"0"	"1"	"0"
VD	"1"	"1"	"1"

FIG. 65(h)

⑧

	BL1	BL2	BL3
WD	"0"	"1"	"0"
VD	"0"	"1"	"0"

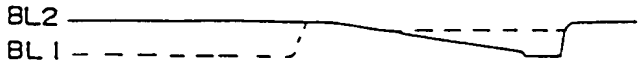


FIG. 66(a)

	BL1	BL2	BL3
WD	"1"	"0"	"1"
VD	"1"	"1"	"1"

FIG. 66(b)

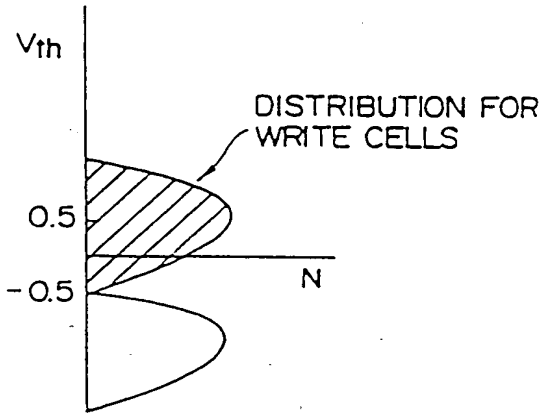
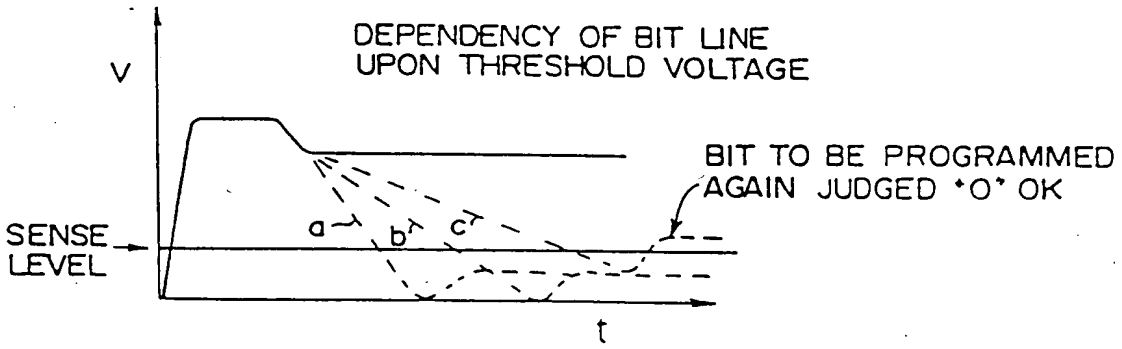


FIG. 66(c)



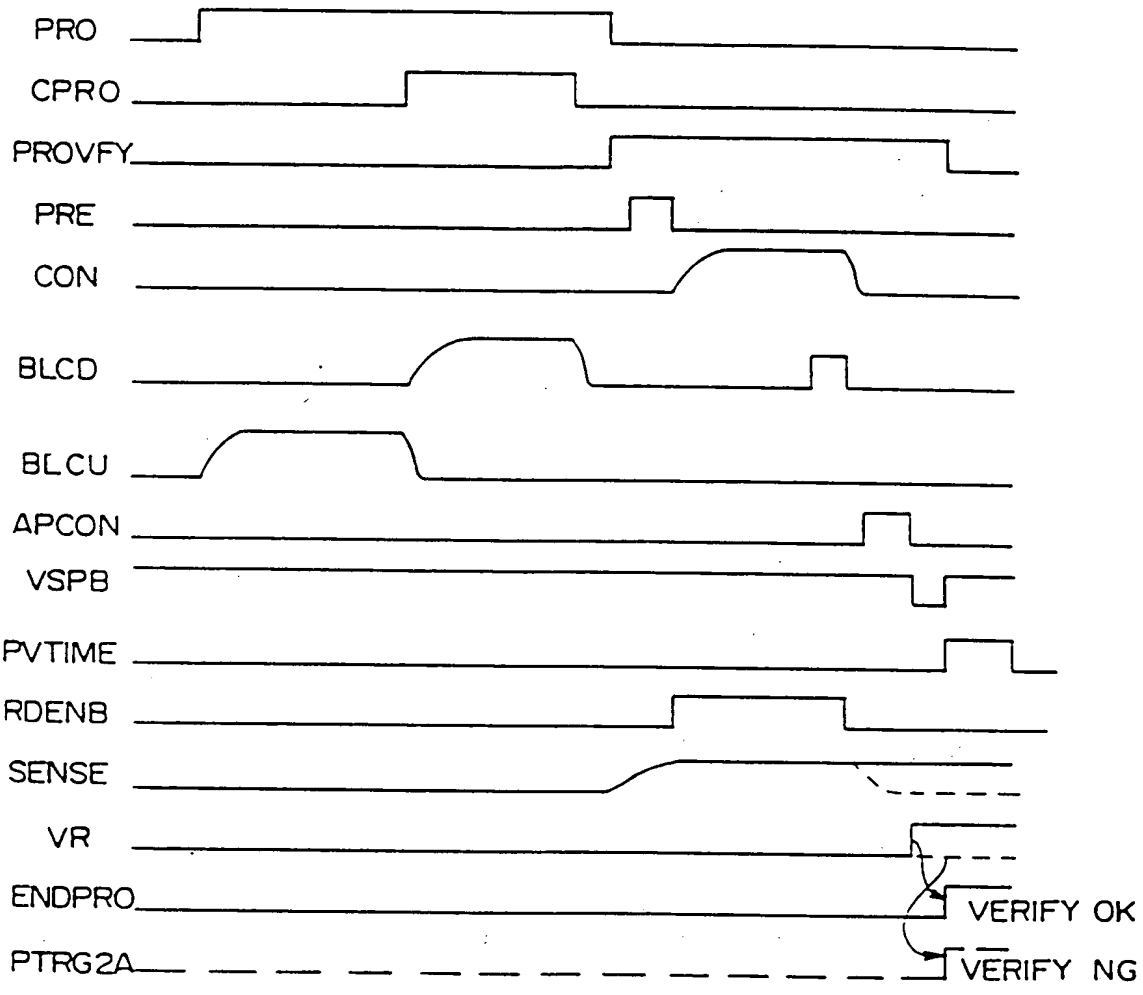

PRO
CPRO
PROVFY
PRE
CON
BLCD
BLCU
APCON
VSPB
PVTIME
RDENB
SENSE
VR
ENDPRO
PTRG2A
VERIFY OK
VERIFY NG

FIG. 67

FIG. 68(a)

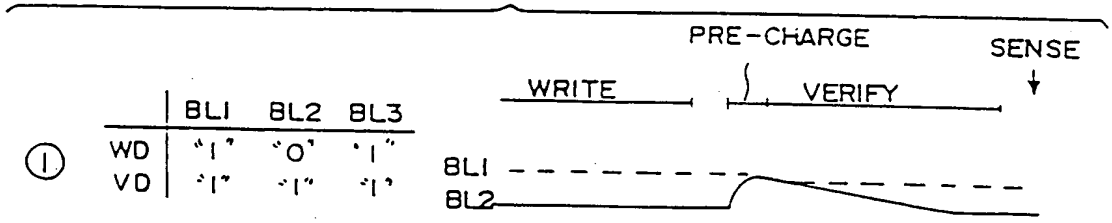


FIG. 68(b)

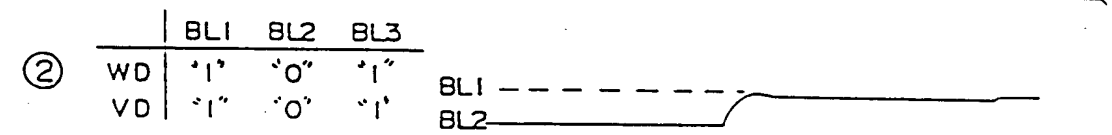


FIG. 68(c)

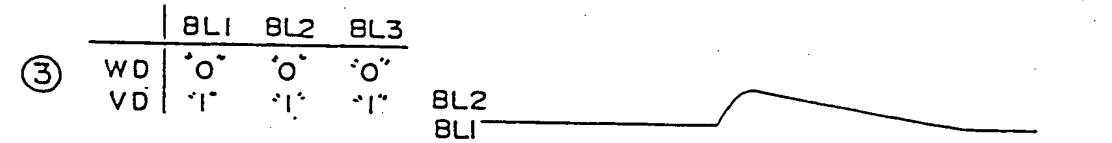


FIG. 68(d)

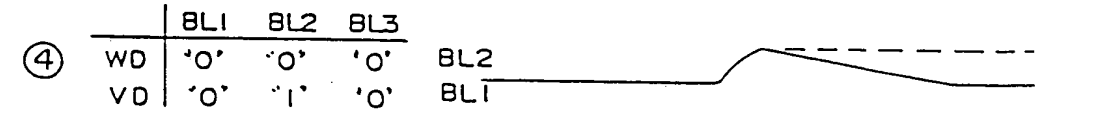


FIG. 68(e)

		BL1	BL2	BL3
⑤	WD	'0'	'0'	'0'
	VD	'1'	'0'	'1'

FIG. 68(f)

		BL1	BL2	BL3
⑥	WD	'0'	'0'	'0'
	VD	'0'	'0'	'0'

FIG. 68(g)

		BL1	BL2	BL3
⑦	WD	'0'	'1'	'0'
	VD	'1'	'1'	'1'

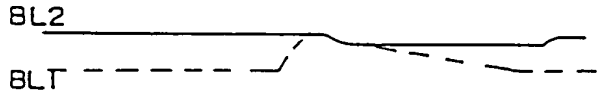


FIG. 68(h)

		BL1	BL2	BL3
⑧	WD	'0'	'1'	'0'
	VD	'0'	'1'	'0'

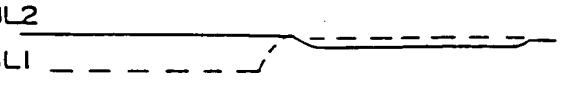


FIG. 69(a)

	BL1	BL2	BL3
WD	"1"	"0"	"1"
VD	"1"	"1"	"1"

FIG. 69(b)

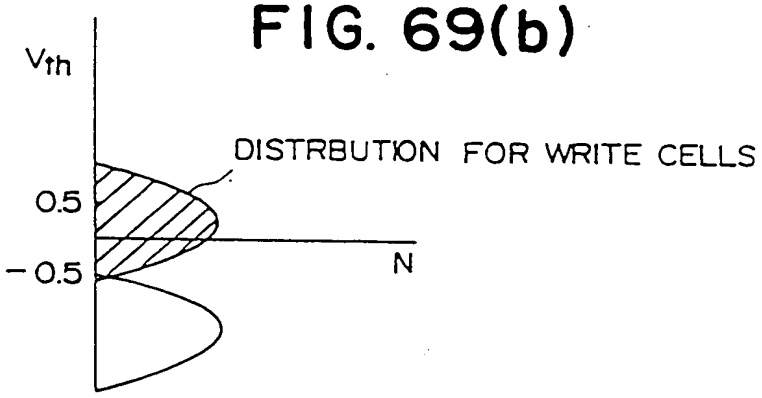


FIG. 69(c)

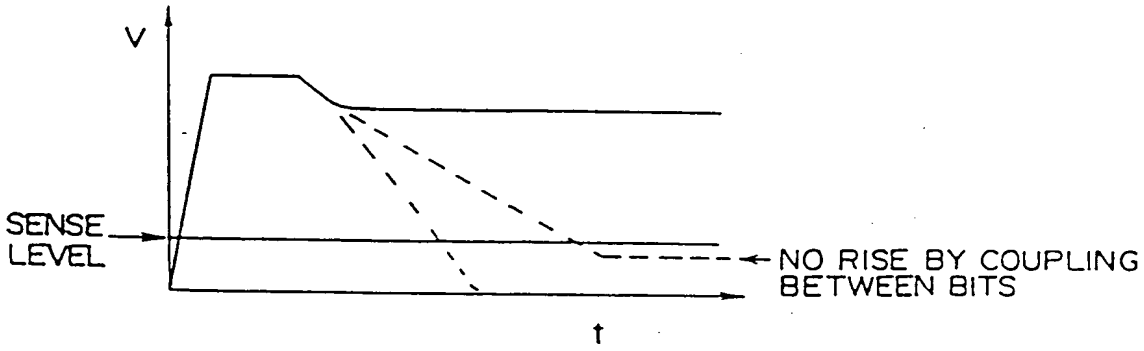


FIG. 70(a)

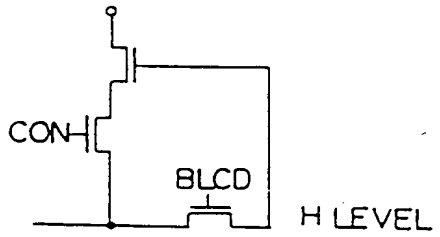


FIG. 70(b)

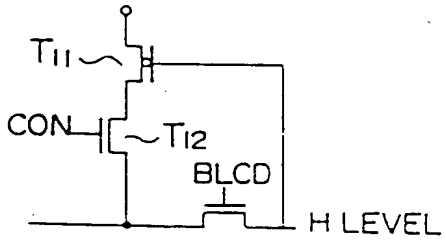
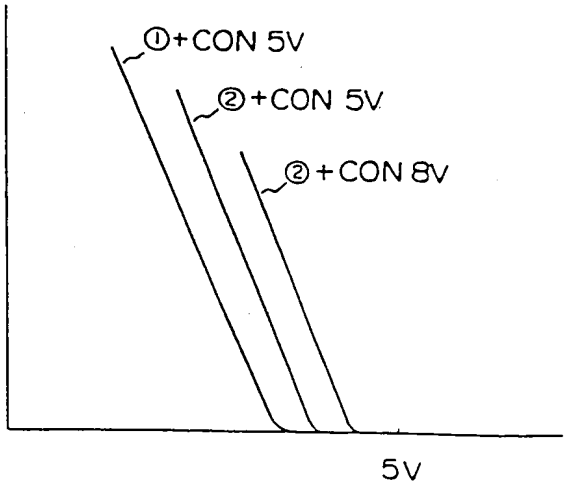


FIG. 70(c)



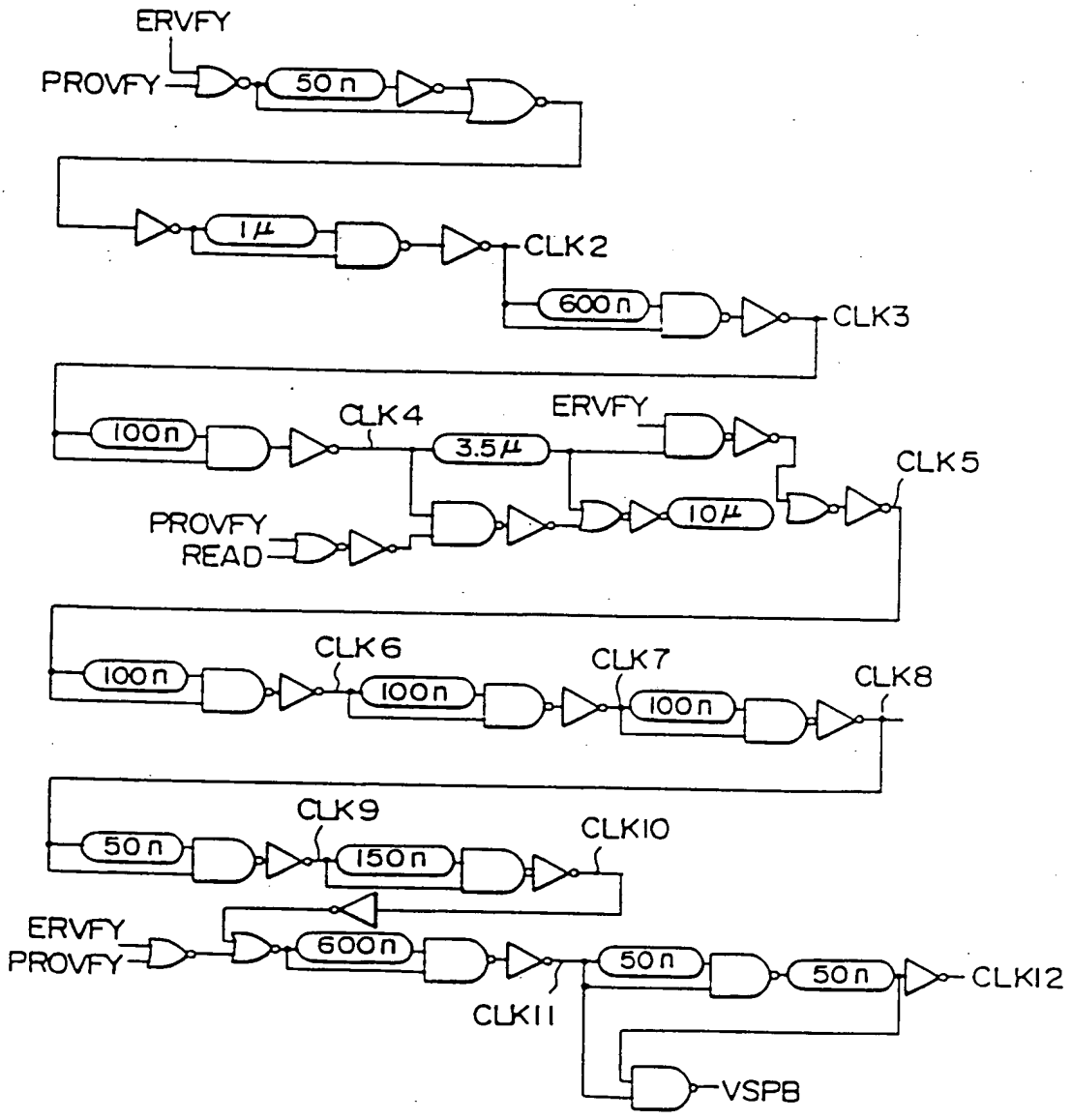

ERVFY
PROVFY
50 n
1 μ
CLK2
600 n
CLK3
100n
CLK4
3.5 μ
ERVFY
CLK5
10 μ
PROVFY
READ
CLK6
100n
CLK7
100n
100n
CLK8
CLK9
50 n
150n
CLK10
ERVFY
PROVFY
600n
50 n
50 n
CLK12
CLK11
VSP8

FIG. 71

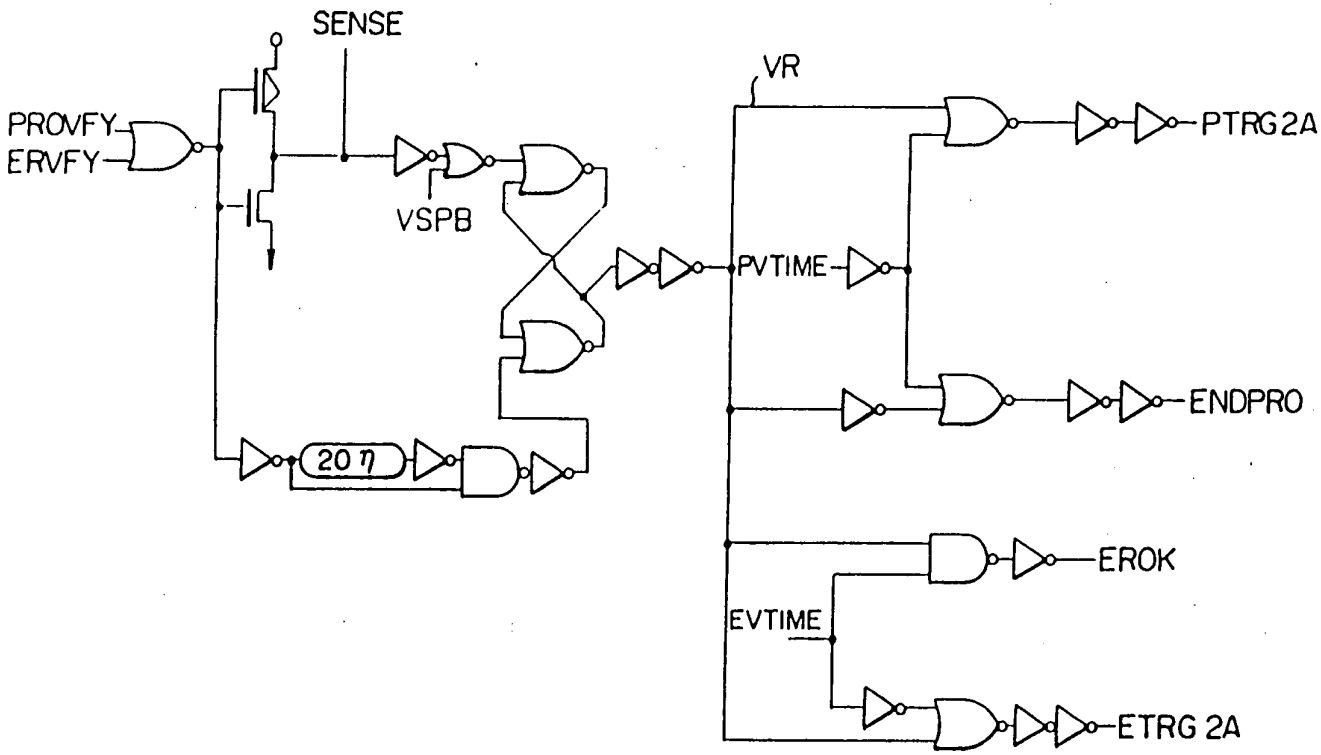


FIG. 72

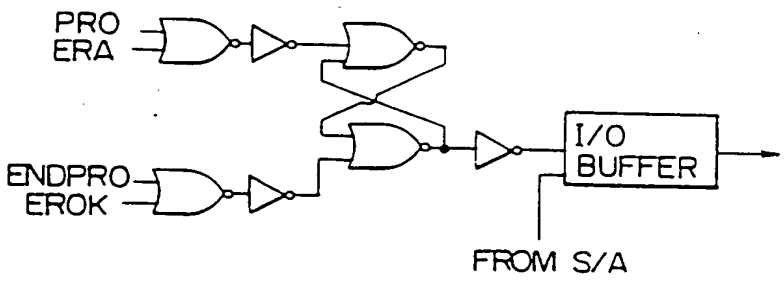


FIG. 73

FIG. 74(a)

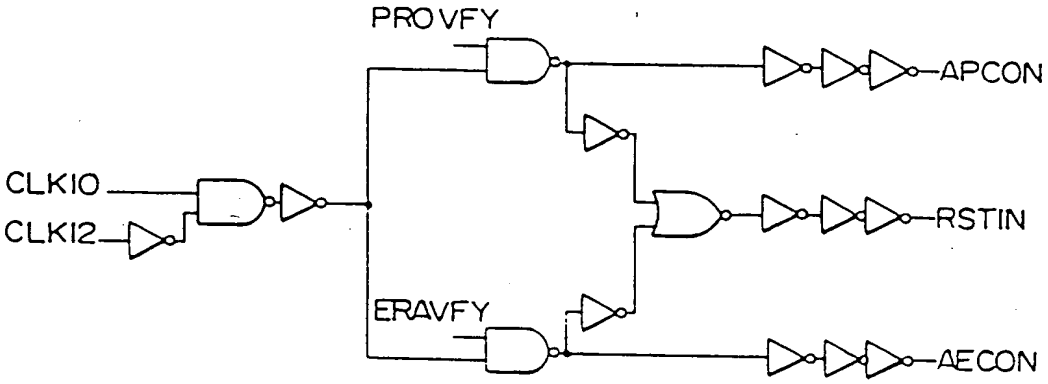


FIG. 74(b)

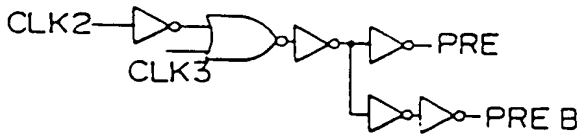
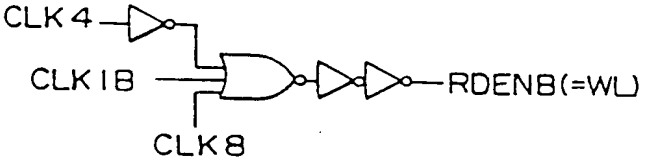


FIG. 74(c)



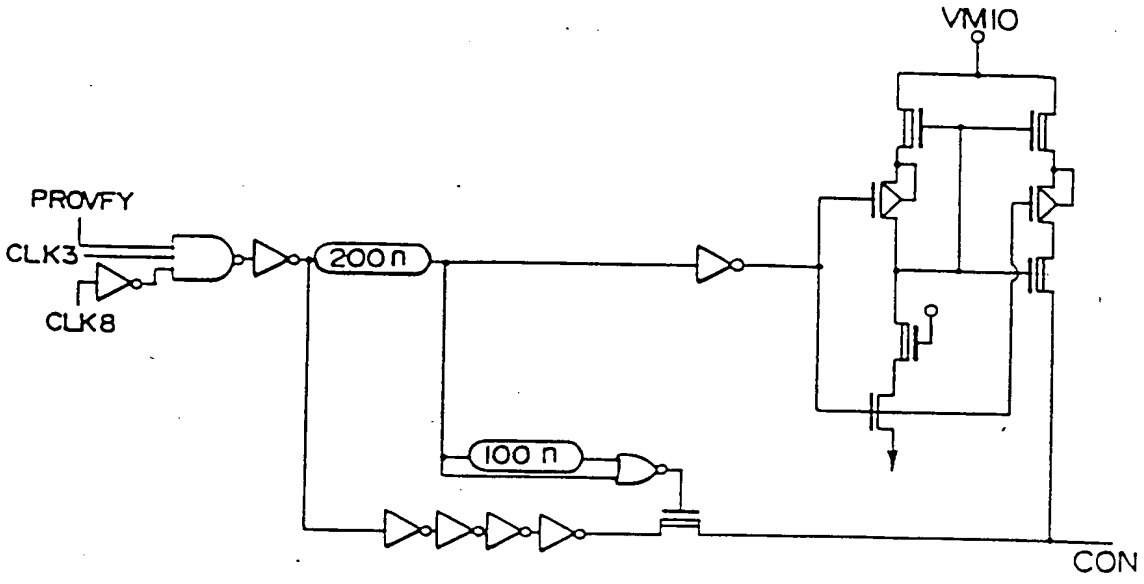


FIG. 75

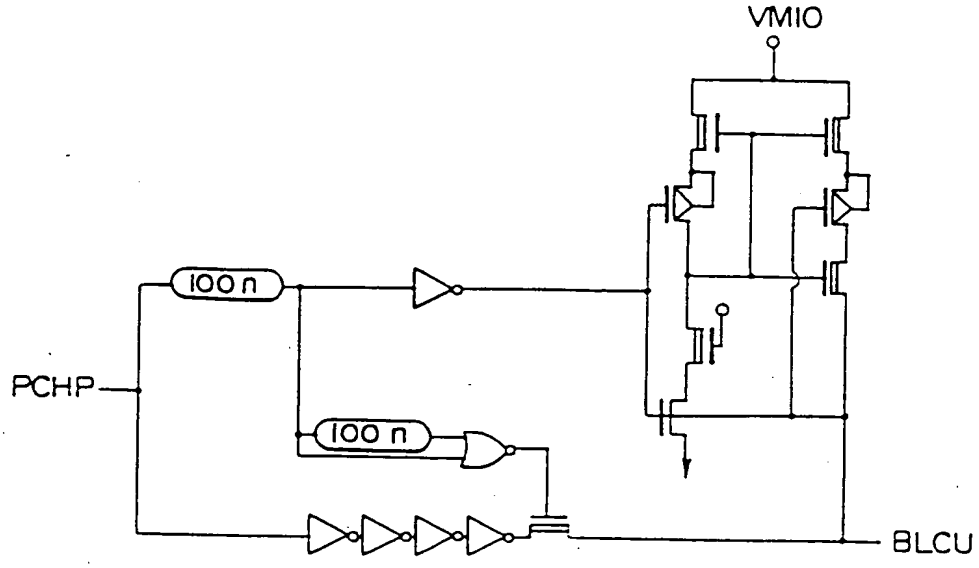


FIG. 76

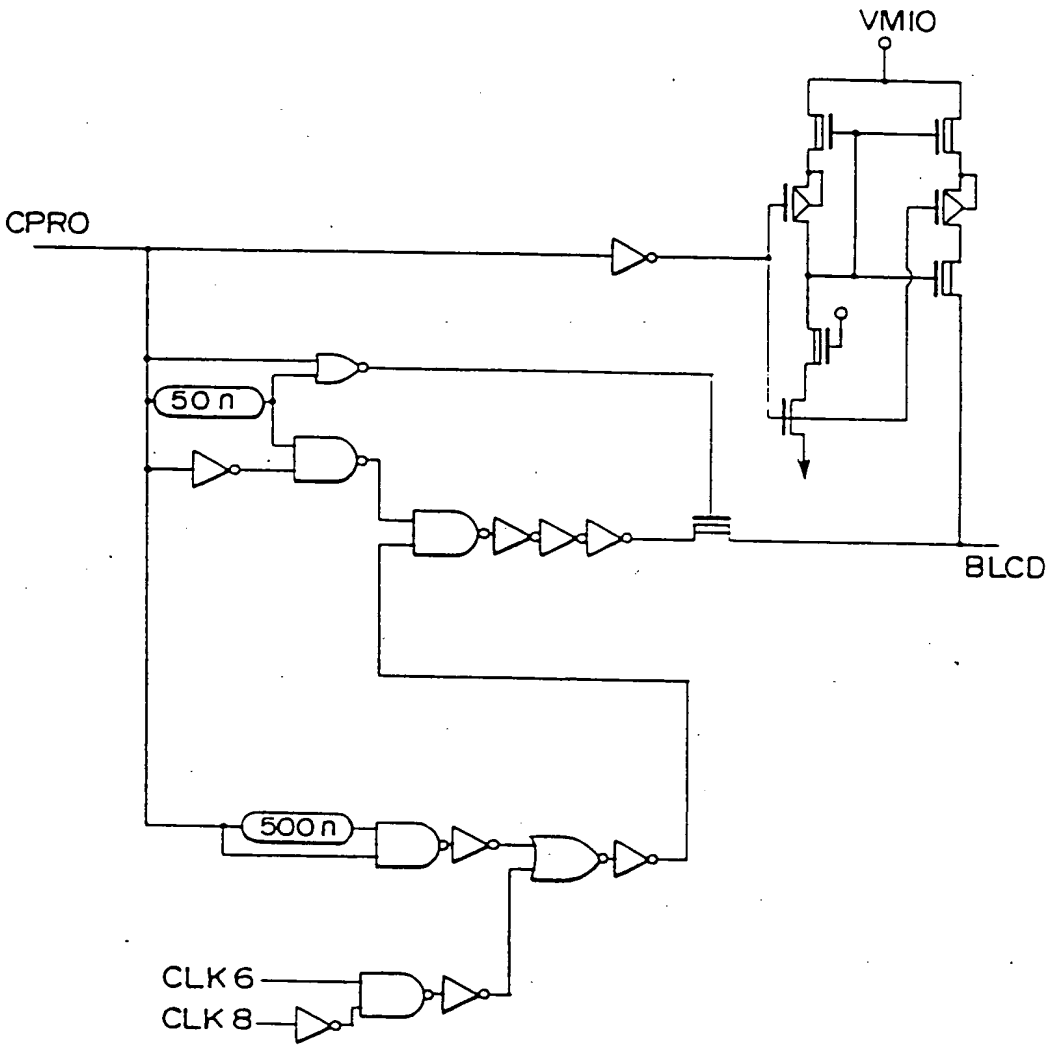


FIG. 77

FIG. 78(a)

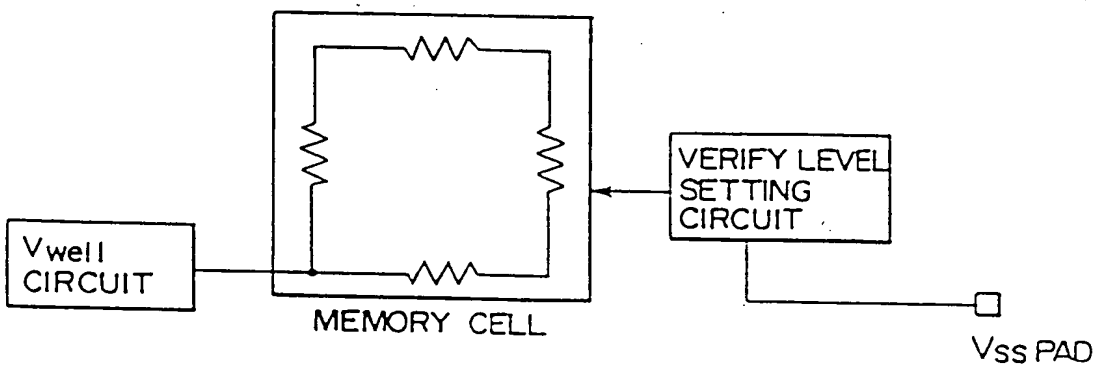
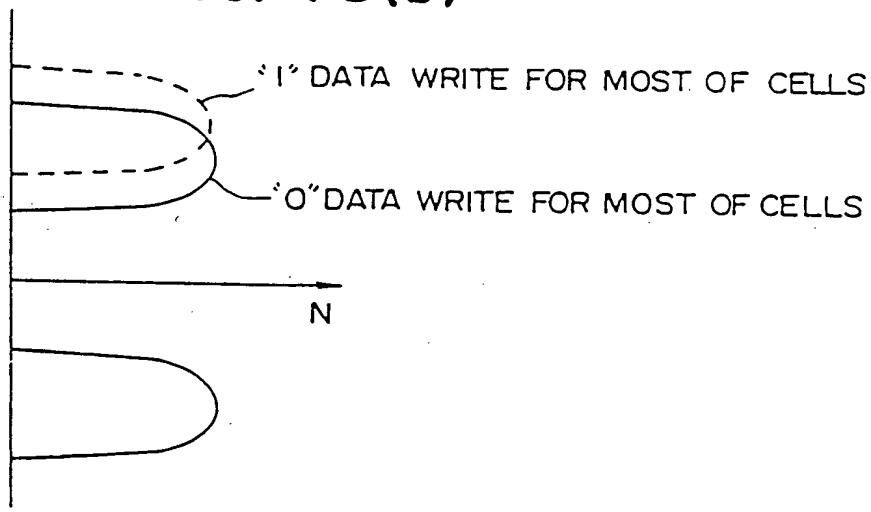


FIG. 78(b)



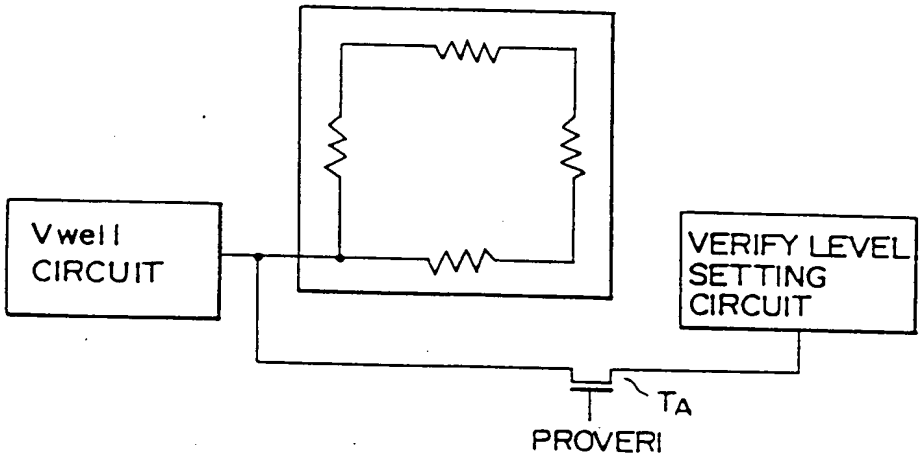


FIG. 79

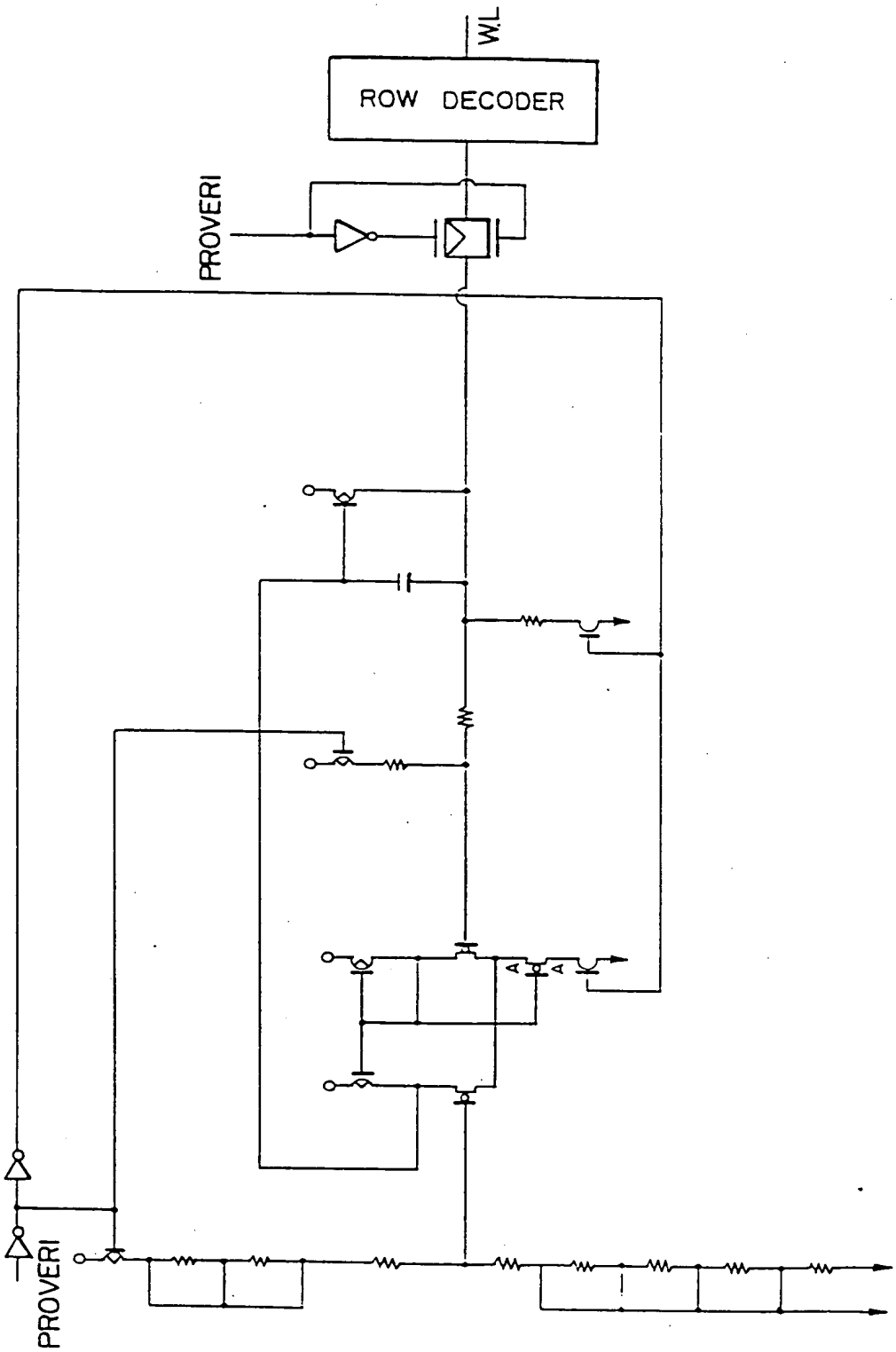


FIG. 80

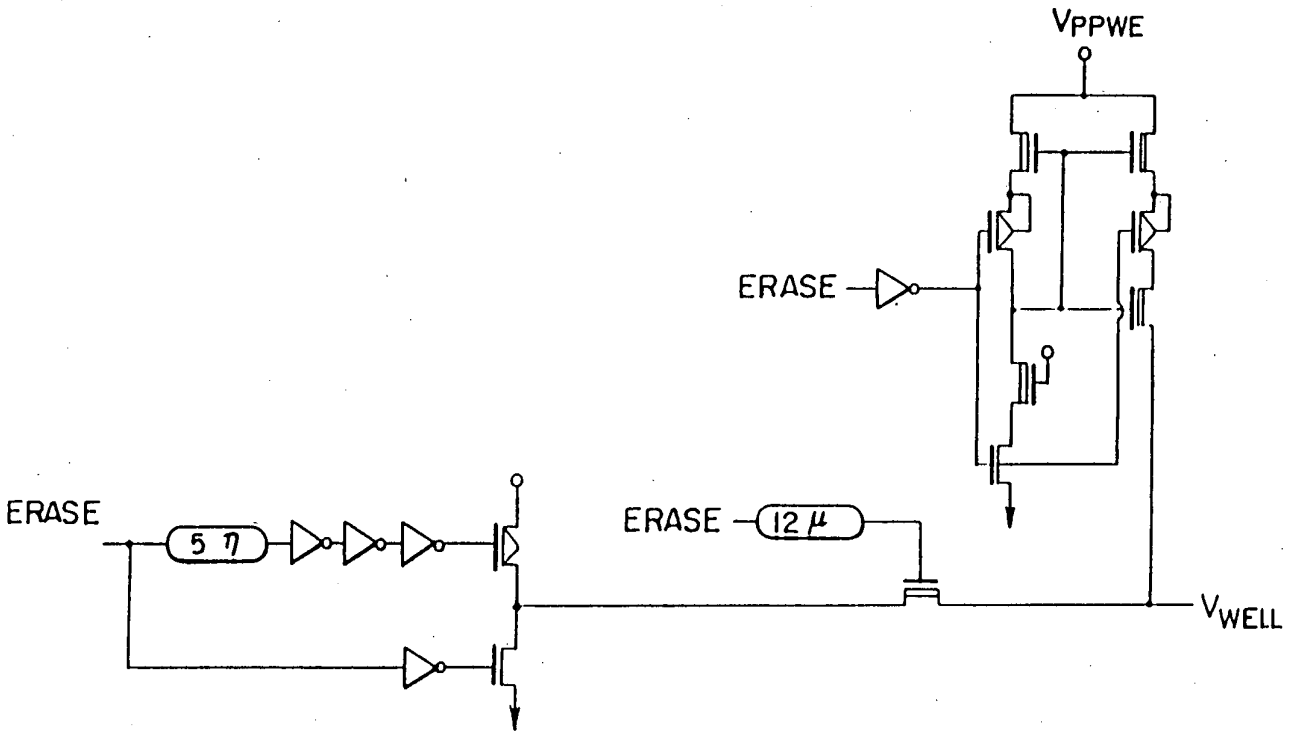


FIG. 81

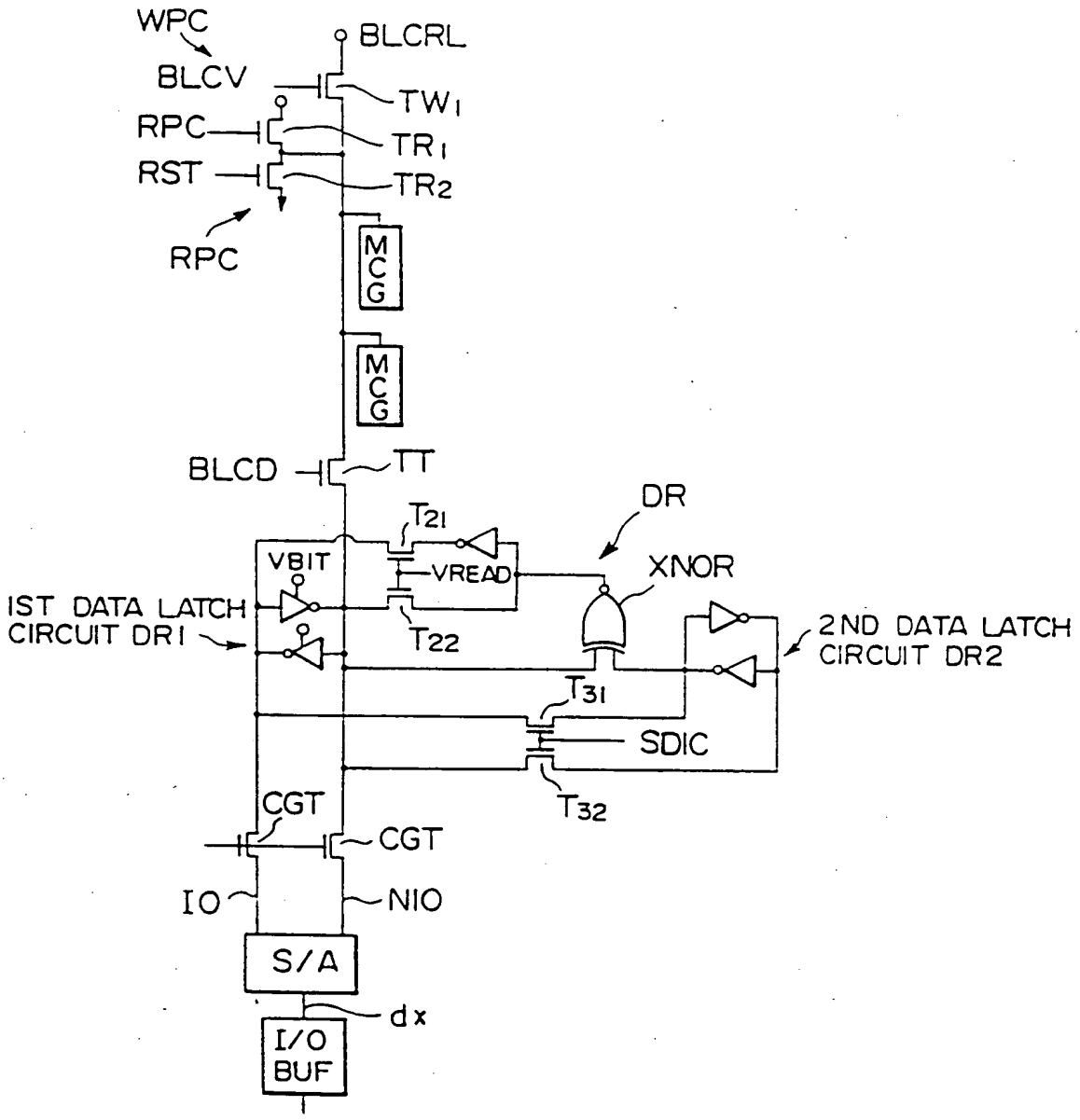


FIG. 82

WRITE DATA	0	0	1	1
VERIFY DATA	0	1	0	1
OUTPUT DATA AFTER COMPARISON	0	1	1	0

FIG. 83

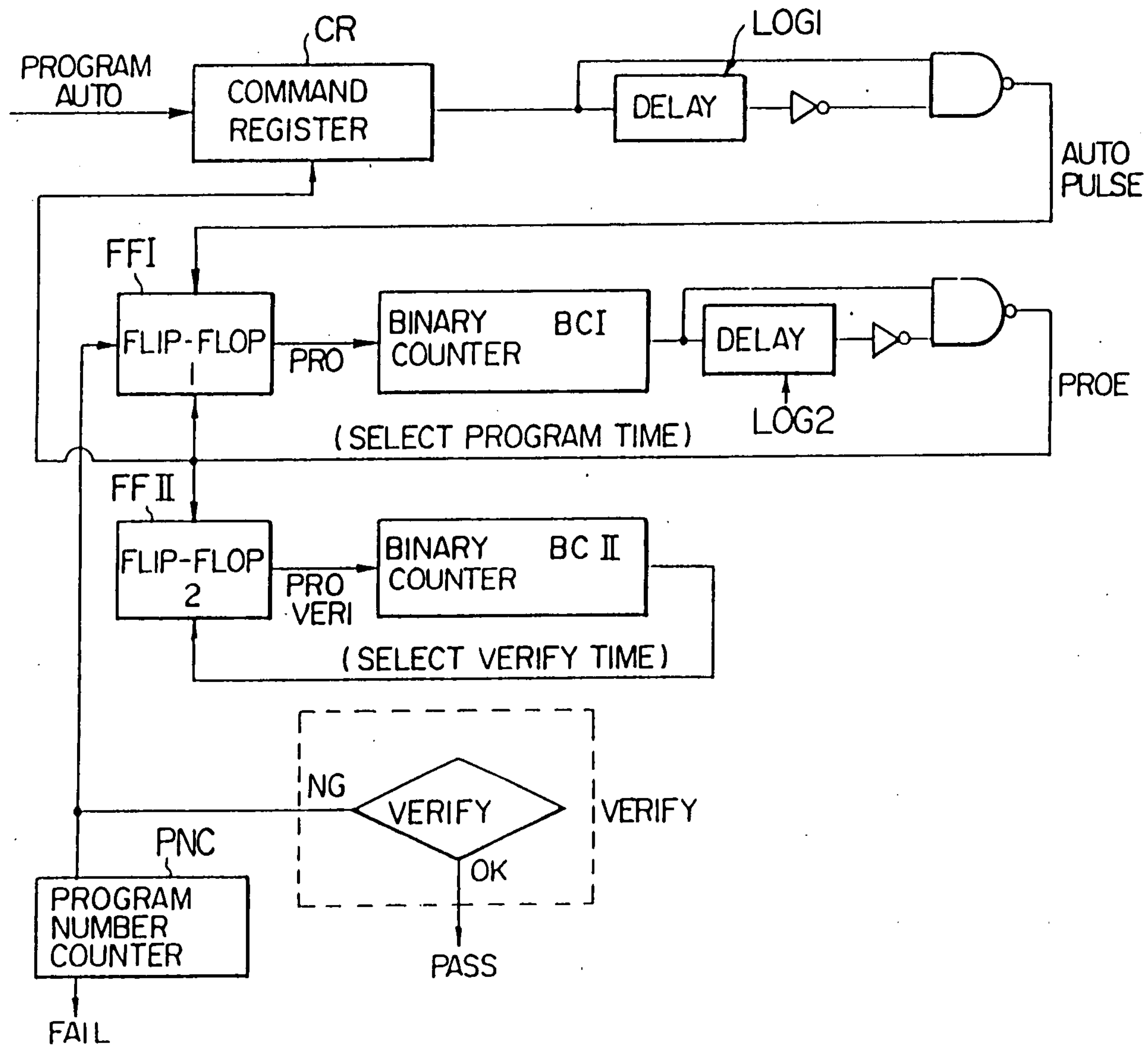

PROGRAM AUTO
CR
COMMAND REGISTER
LOGI
DELAY
AUTO PULSE
FFI
FLIP-FLOP I
PRO
BINARY COUNTER
BCI
DELAY
LOG2
PROE
(SELECT PROGRAM TIME)
FF II
FLIP-FLOP 2
PRO VERI
BINARY COUNTER
BC II
(SELECT VERIFY TIME)
NG
VERIFY
OK
VERIFY
PASS
PNC
PROGRAM NUMBER COUNTER
FAIL

FIG. 84

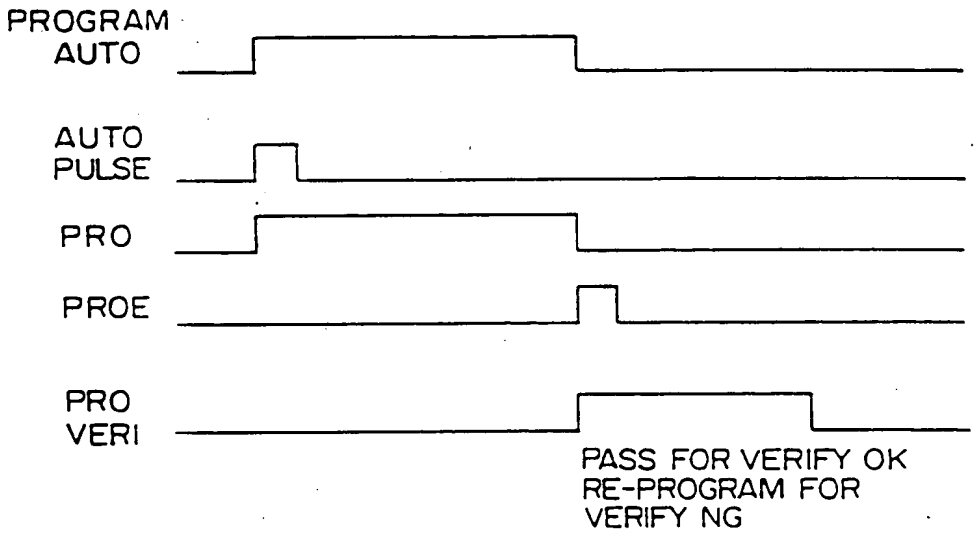

PROGRAM
AUTO
AUTO
PULSE
PRO
PROE
PRO
VERI
PASS FOR VERIFY OK
RE-PROGRAM FOR
VERIFY NG

FIG. 85

PROGRAM & PROGRAM VERIFY OPERATIONS

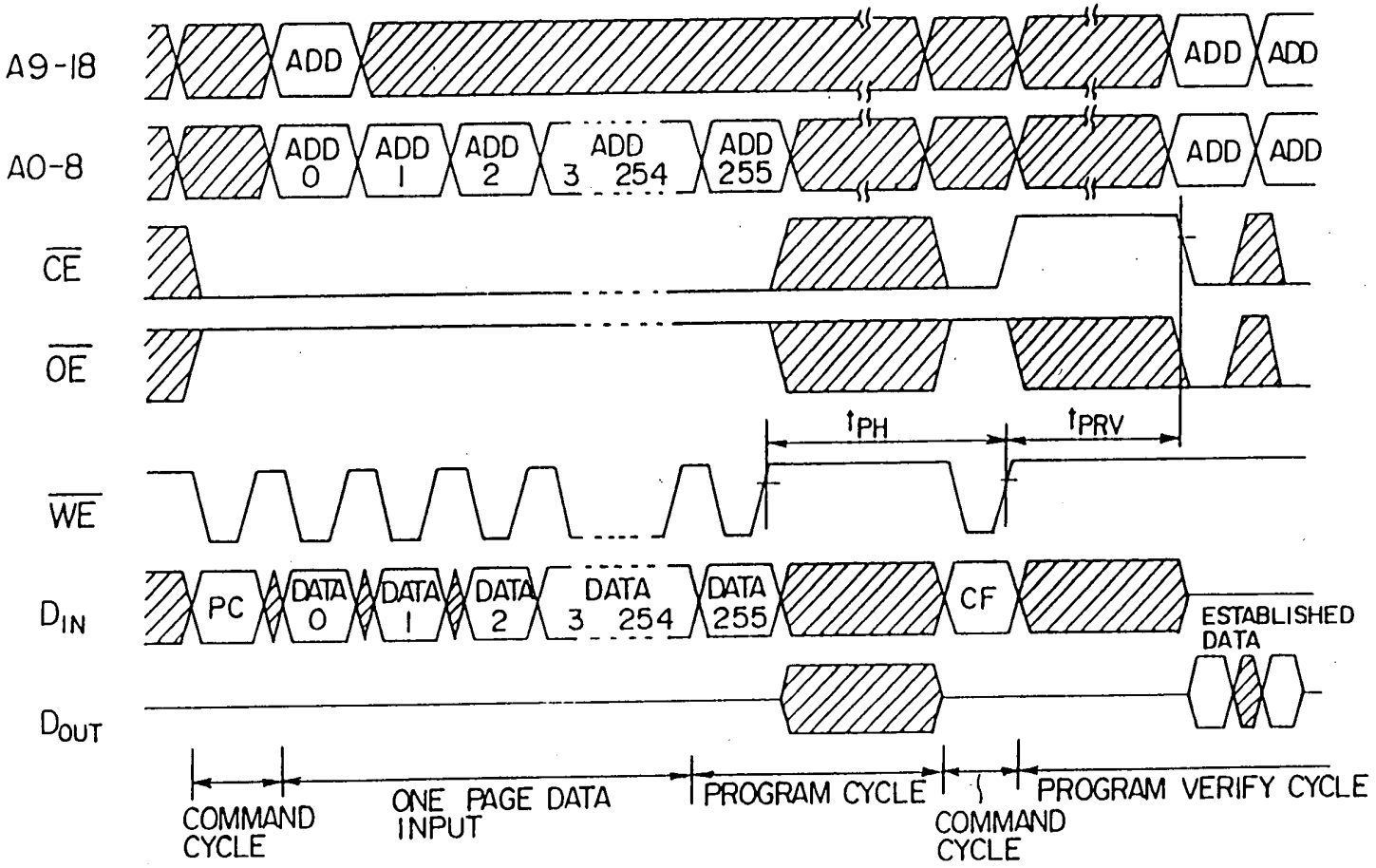


FIG. 86

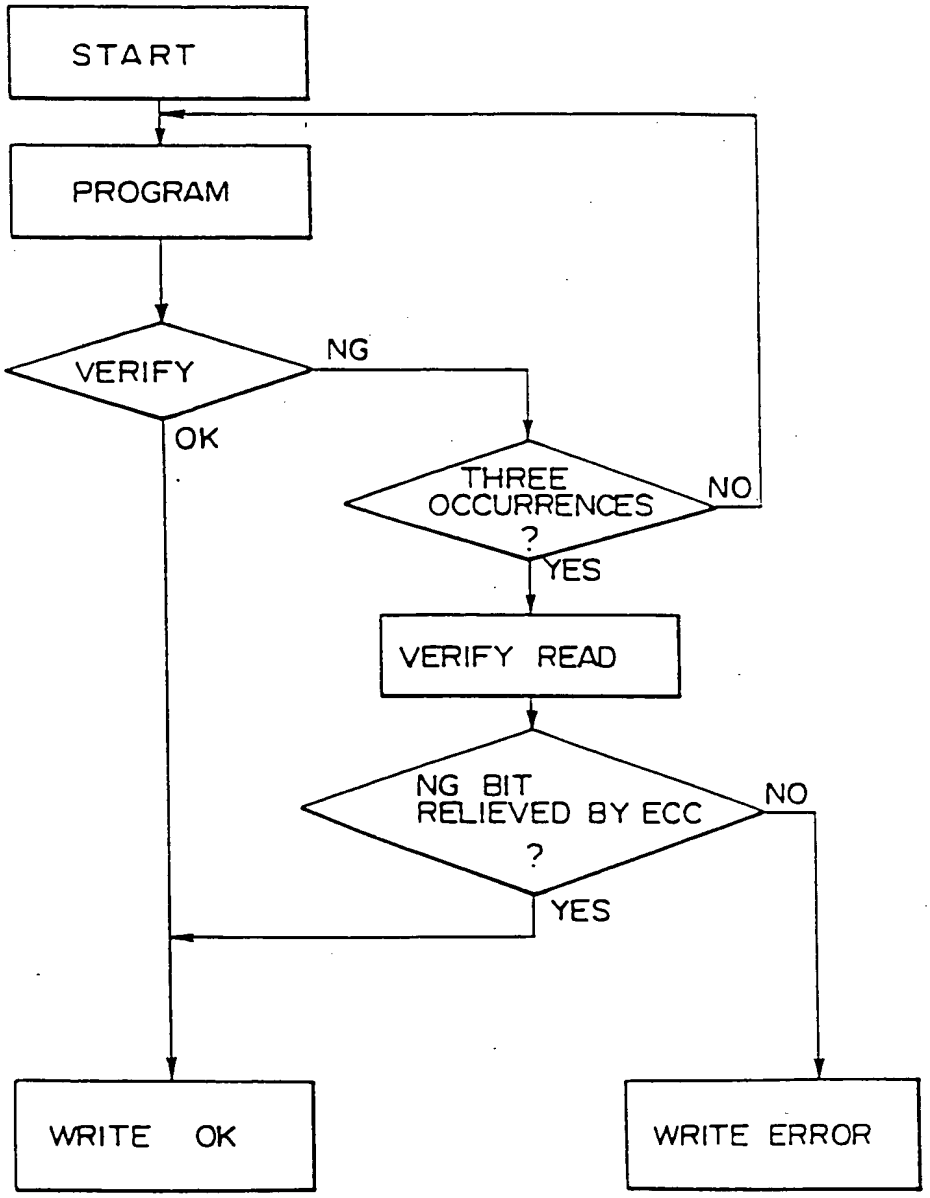

START
PROGRAM
VERIFY
NG
OK
THREE OCCURRENCES ?
NO
YES
VERIFY READ
NG BIT RELIEVED BY ECC ?
NO
YES
WRITE OK
WRITE ERROR

FIG. 87

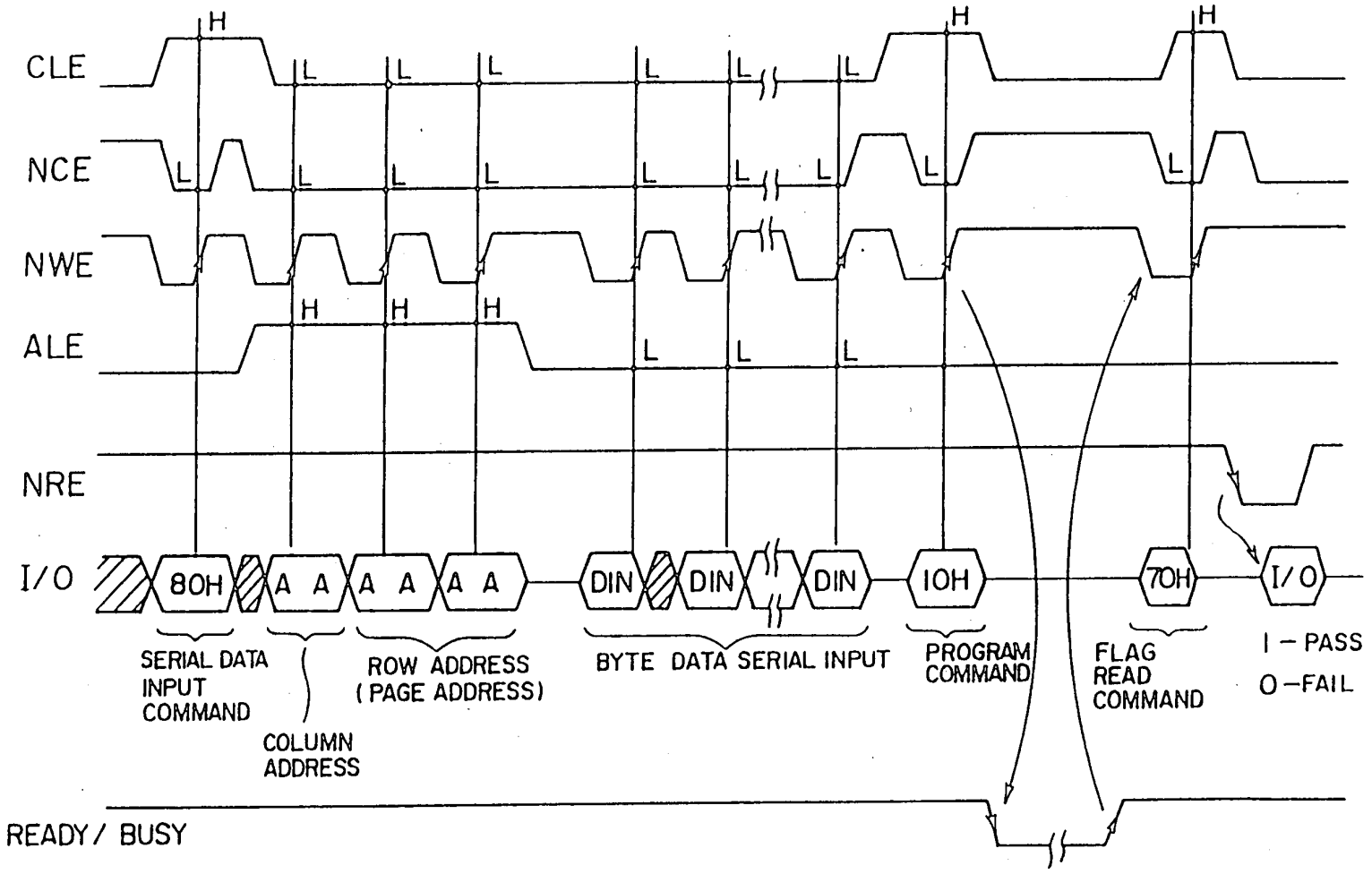

CLE
NCE
NWE
ALE
NRE
I/O
READY/ BUSY
H
L
80H
A A
A A
A A
DIN
DIN
DIN
10H
70H
I/O
SERIAL DATA INPUT COMMAND
COLUMN ADDRESS
ROW ADDRESS (PAGE ADDRESS)
BYTE DATA SERIAL INPUT
PROGRAM COMMAND
FLAG READ COMMAND
I - PASS
O - FAIL

FIG.88

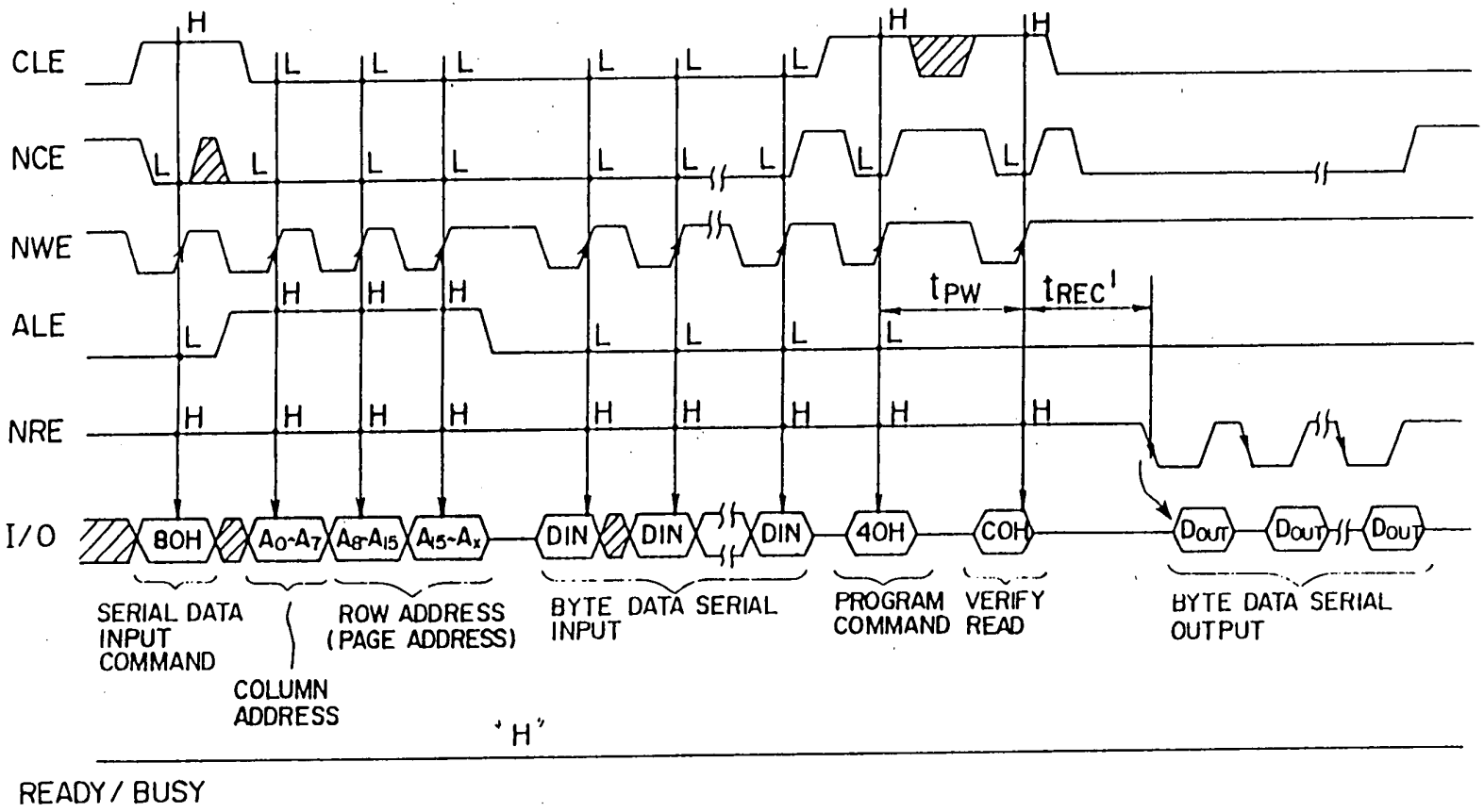

CLE
NCE
NWE
ALE
NRE
I/O
READY/BUSY
80H
A0~A7
A8~A15
A15~Ax
DIN
DIN
DIN
40H
COH
DOUT
DOUT
DOUT
tPW
tREC'
SERIAL DATA INPUT COMMAND
COLUMN ADDRESS
ROW ADDRESS (PAGE ADDRESS)
BYTE DATA SERIAL INPUT
PROGRAM COMMAND
VERIFY READ
BYTE DATA SERIAL OUTPUT
"H"

FIG.89

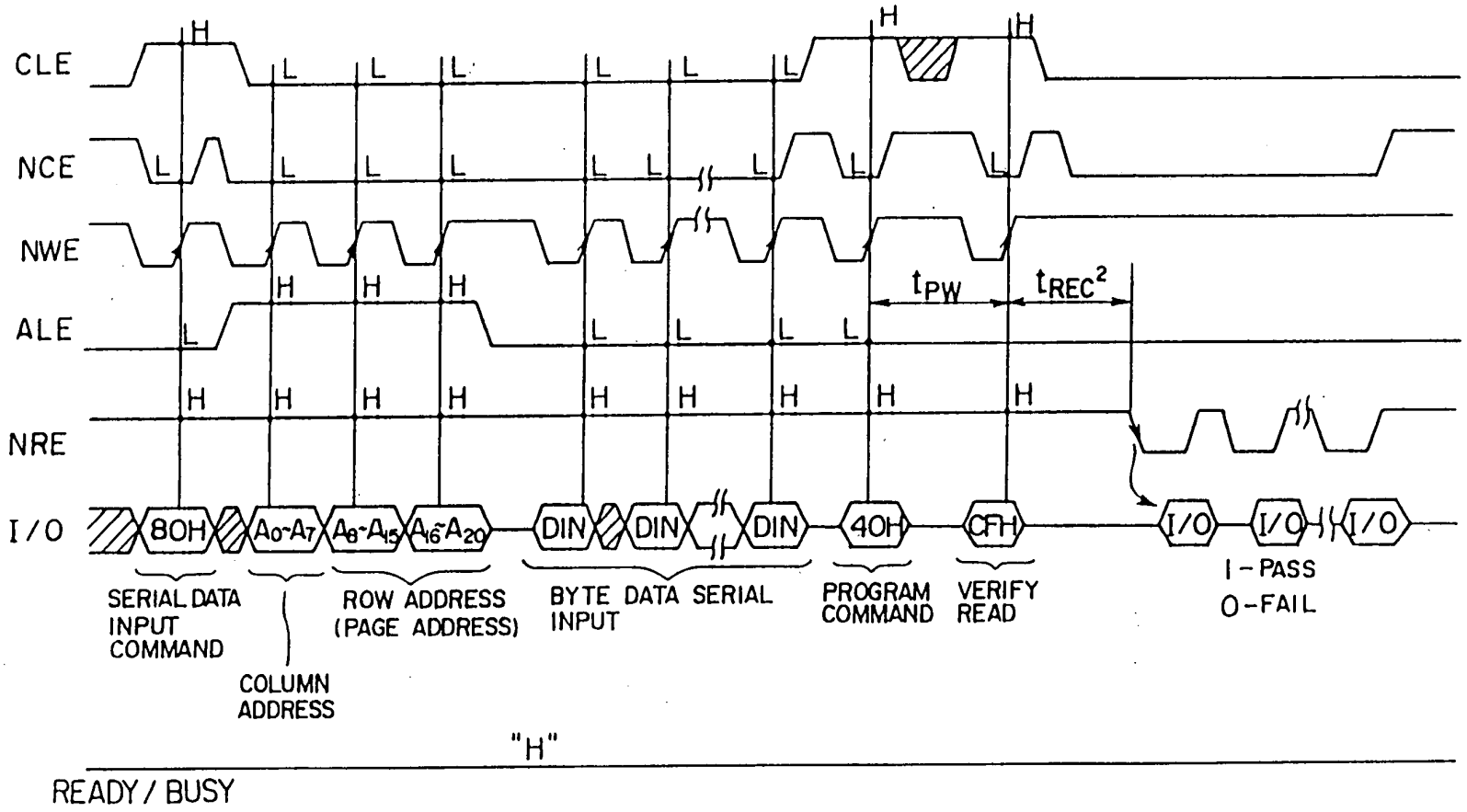

CLE
NCE
NWE
ALE
NRE
I/O
80H
A0-A7
A8-A15
A16-A20
DIN
DIN
DIN
40H
CFH
I/O
I/O
I/O
tPW
tREC2
SERIAL DATA INPUT COMMAND
COLUMN ADDRESS
ROW ADDRESS (PAGE ADDRESS)
BYTE DATA SERIAL INPUT
PROGRAM COMMAND
VERIFY READ
I-PASS
O-FAIL
"H"
READY/BUSY

FIG. 90

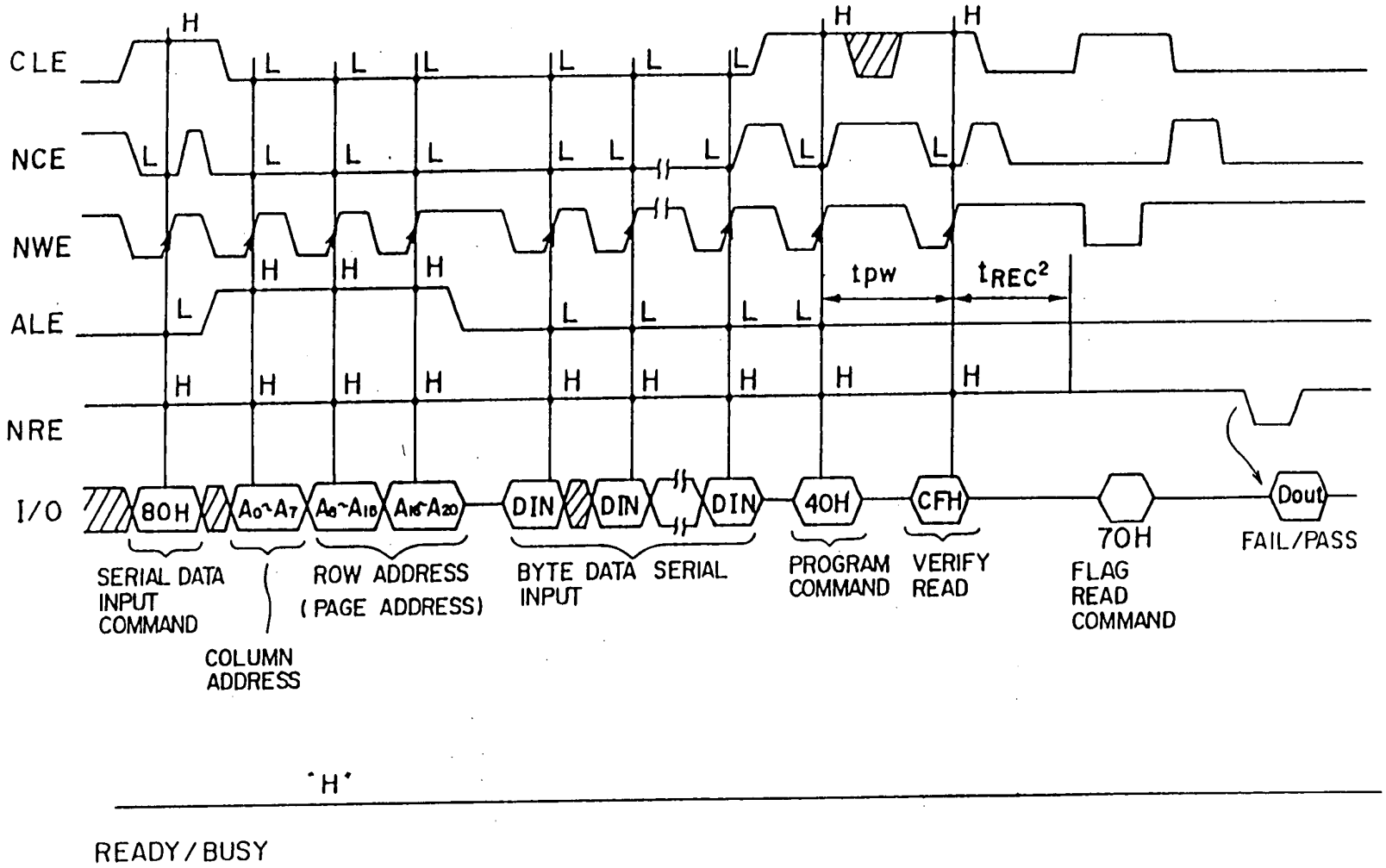

CLE
NCE
NWE
ALE
NRE
I/O
READY/BUSY
"H"
80H
A0~A7
A8~A15
A16~A20
DIN
DIN
DIN
40H
CFH
70H
Dout
tpw
tREC2
SERIAL DATA INPUT COMMAND
COLUMN ADDRESS
ROW ADDRESS (PAGE ADDRESS)
BYTE DATA SERIAL INPUT
PROGRAM COMMAND
VERIFY READ
FLAG READ COMMAND
FAIL/PASS

FIG. 91

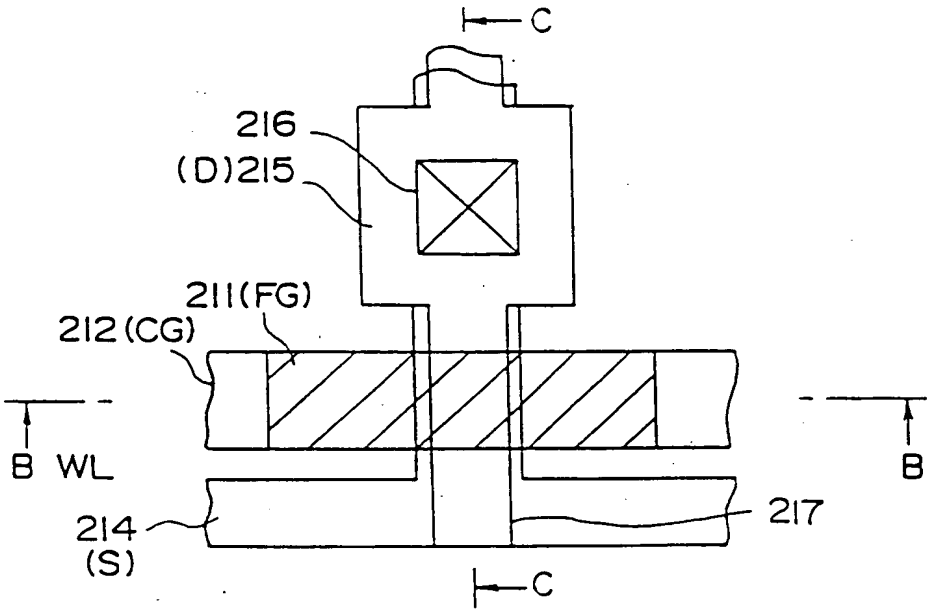


FIG. 92

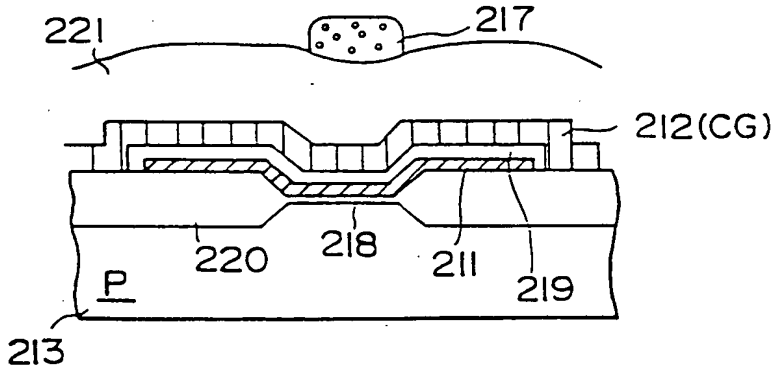


FIG. 93

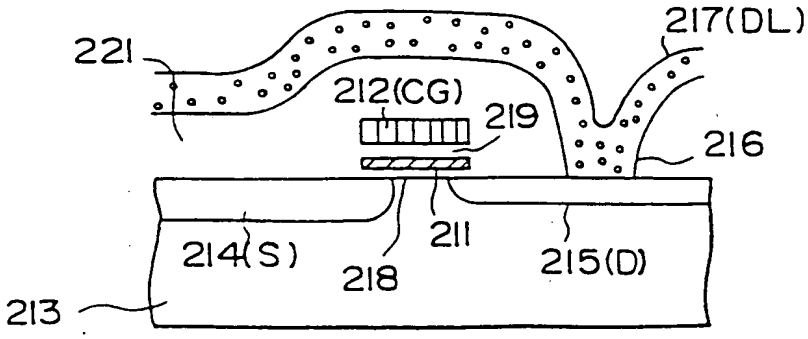


FIG. 94

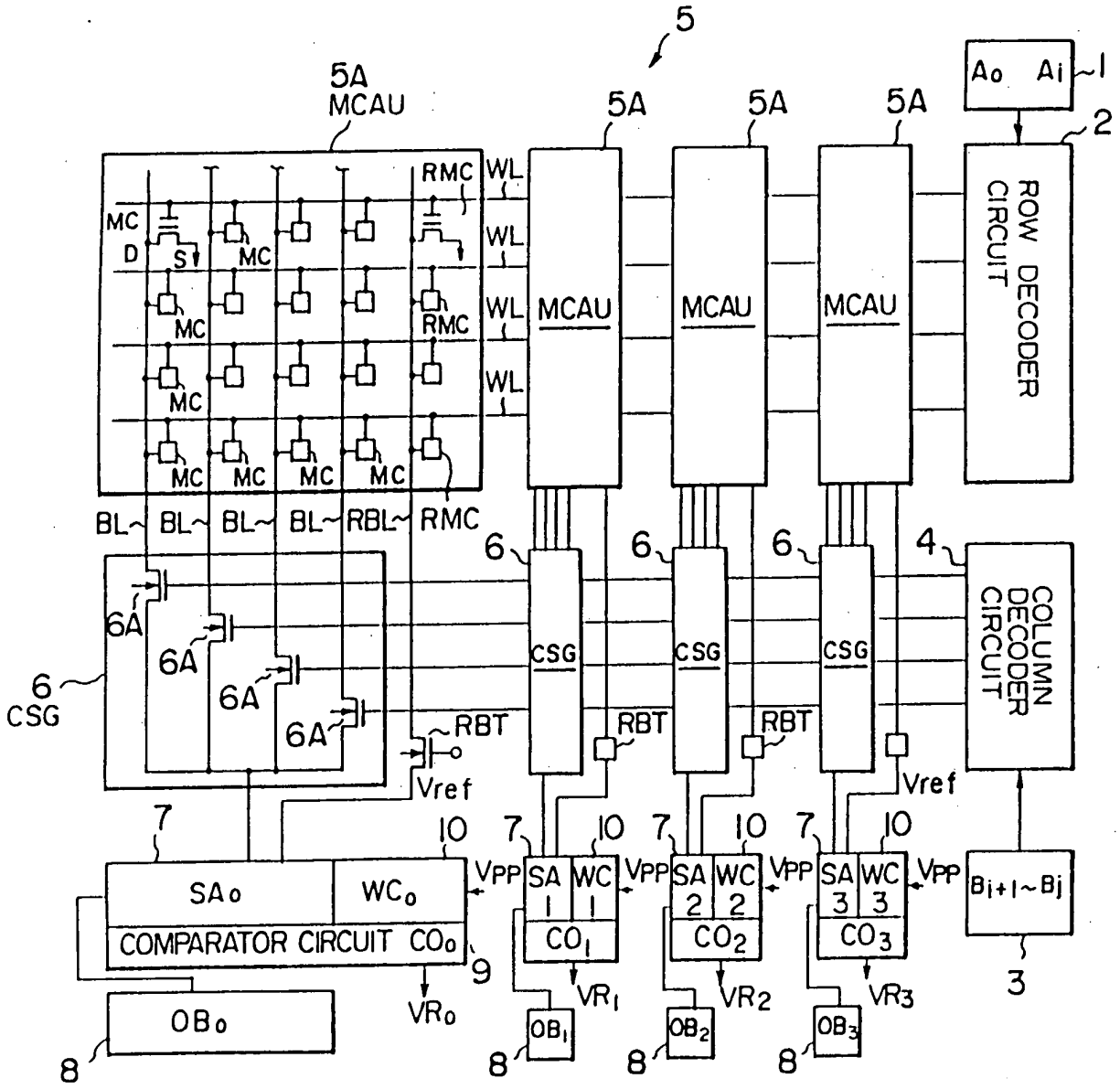

5
5A
MCAU
5A
5A
5A
A0 Ai
1
2
ROW DECODER CIRCUIT
RMC
WL
MC
D
S
MCAU
MCAU
MCAU
BL
RBL
6
6A
CSG
RBT
Vref
4
COLUMN DECODER CIRCUIT
7
10
SA0
WC0
COMPARATOR CIRCUIT CO0
9
VPP
SA 1
WC 1
SA 2
WC 2
SA 3
WC 3
CO1
CO2
CO3
VR0
VR1
VR2
VR3
OB0
OB1
OB2
OB3
8
Bi+1~Bj
3

FIG. 95

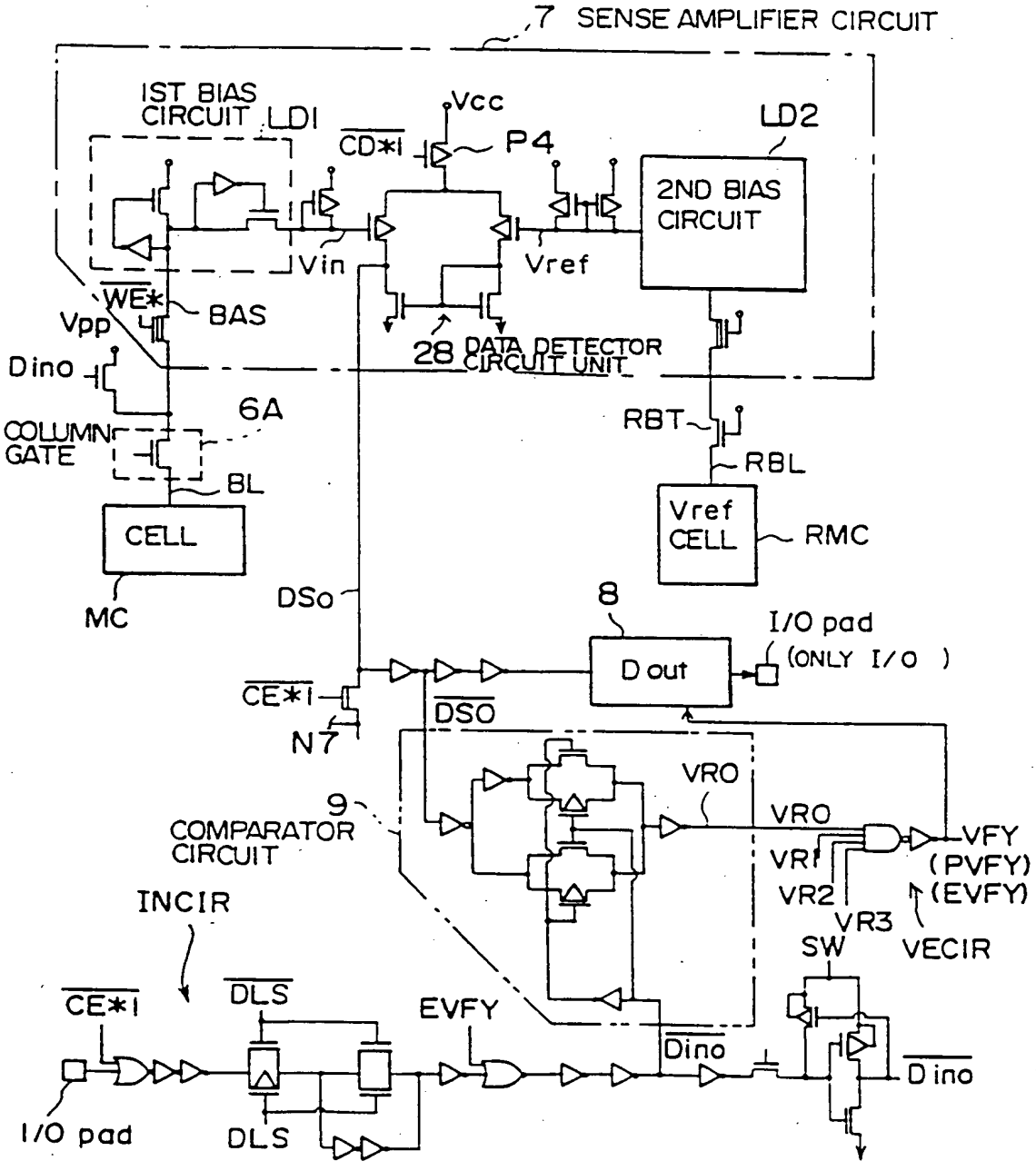

7 SENSE AMPLIFIER CIRCUIT
IST BIAS CIRCUIT
LD1
Vcc
CD*I
P4
LD2
2ND BIAS CIRCUIT
Vin
Vref
WE*
BAS
Vpp
28 DATA DETECTOR CIRCUIT UNIT
Dino
6A
COLUMN GATE
BL
CELL
MC
RBT
RBL
Vref CELL
RMC
DSo
8
D out
I/O pad
(ONLY I/O)
CE*I
N7
DSO
9
COMPARATOR CIRCUIT
VRO
VRO
VFY
(PVFY)
(EVFY)
VR1
VR2
VR3
SW
VECIR
INCIR
CE*I
DLS
EVFY
Dino
Dino
I/O pad
DLS

FIG. 96

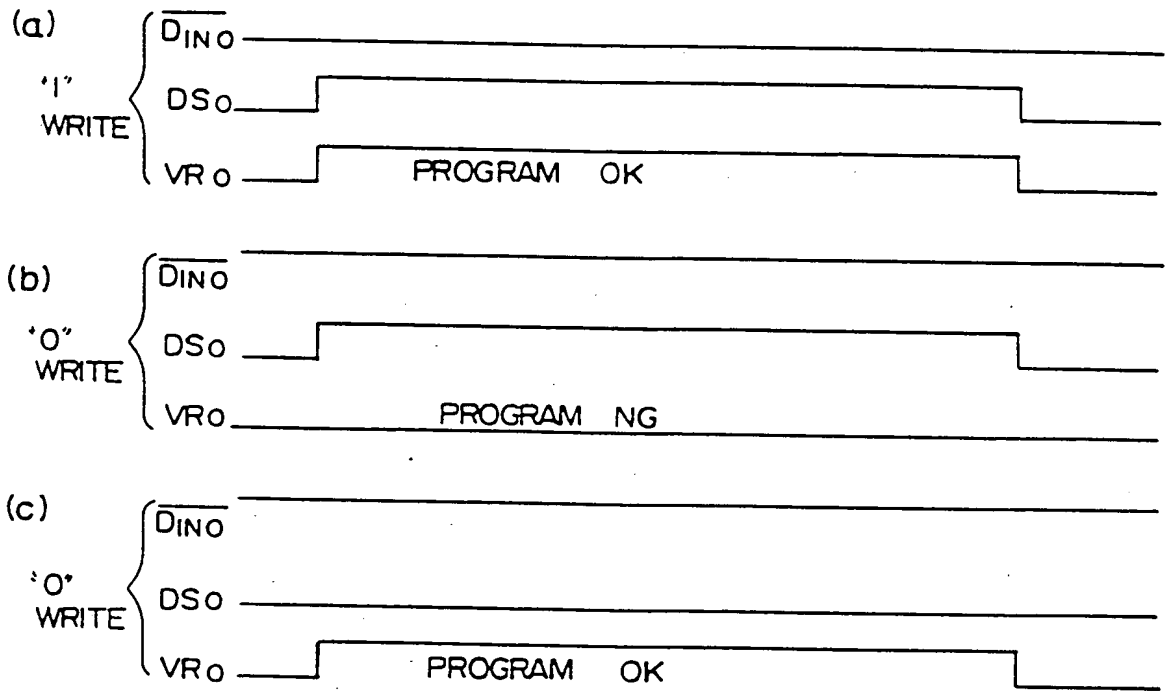

(a)
"1" WRITE
$\overline{D_{IN}}$ o
DSo
VR o
PROGRAM OK
(b)
"0" WRITE
$\overline{D_{IN}}$ o
DSo
VRo
PROGRAM NG
(c)
"0" WRITE
$\overline{D_{IN}}$ o
DSo
VRo
PROGRAM OK

FIG. 97

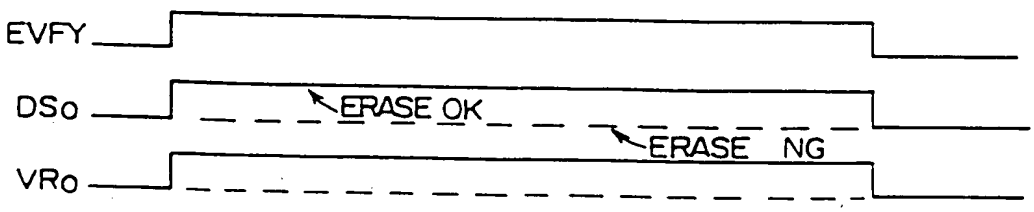

EVFY
DSo
ERASE OK
ERASE NG
VRo

FIG. 98

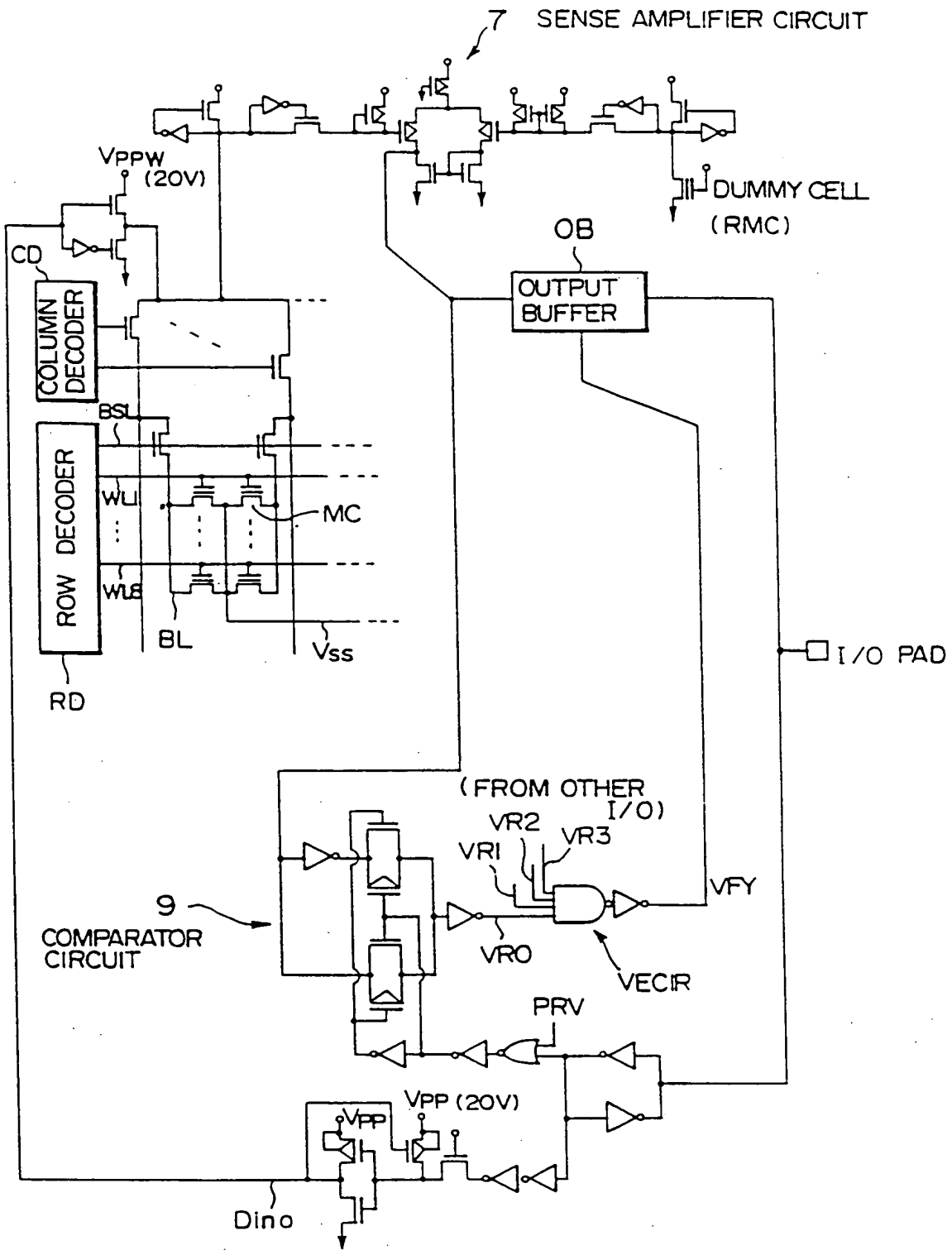

7 SENSE AMPLIFIER CIRCUIT
VPPW (20V)
DUMMY CELL (RMC)
OB
OUTPUT BUFFER
CD
COLUMN DECODER
BSL
ROW DECODER
WL1
WL8
MC
BL
Vss
RD
I/O PAD
(FROM OTHER I/O)
VR2
VR3
VR1
VFY
9
COMPARATOR CIRCUIT
VRO
VECIR
PRV
VPP (20V)
VPP
Dino

FIG. 99

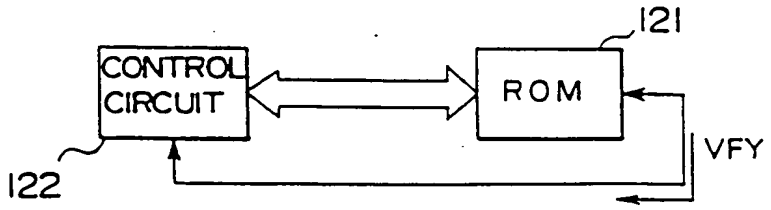


FIG.100

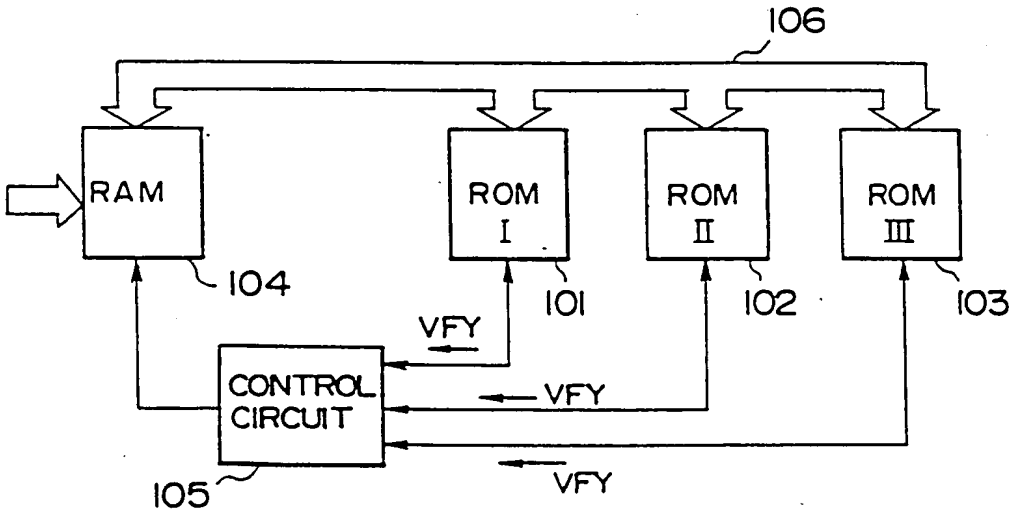


FIG.101

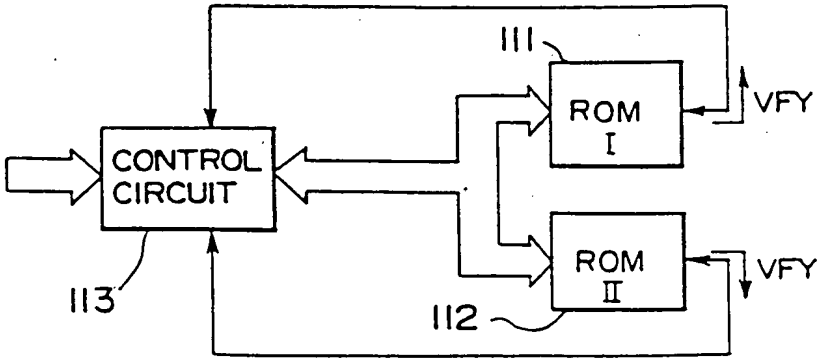


FIG.102

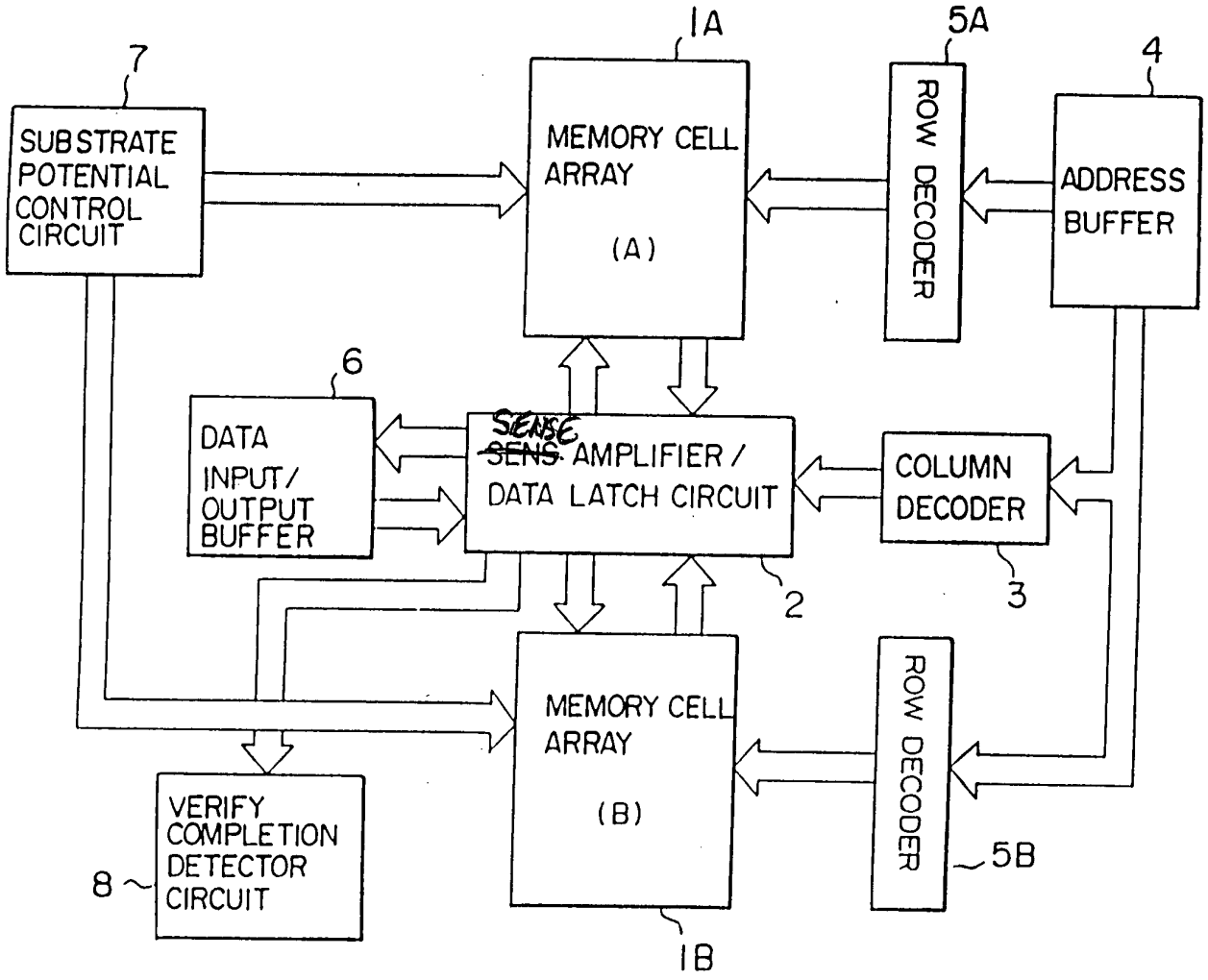

1A
5A
4
7
SUBSTRATE POTENTIAL CONTROL CIRCUIT
MEMORY CELL ARRAY (A)
ROW DECODER
ADDRESS BUFFER
6
DATA INPUT/ OUTPUT BUFFER
SENSE AMPLIFIER / DATA LATCH CIRCUIT
COLUMN DECODER
2
3
MEMORY CELL ARRAY (B)
ROW DECODER
5B
VERIFY COMPLETION DETECTOR CIRCUIT
8
1B

FIG. 53